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FIBER OPTICS TRANSMITTER INTEGRATED CIRCUIT DEVELOPMENT.(U)
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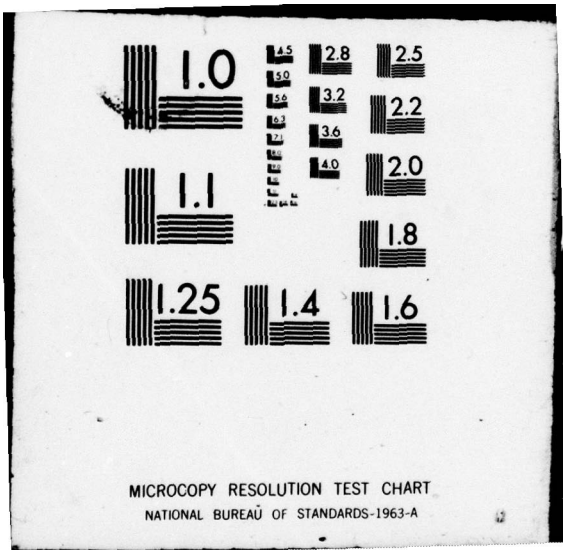
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FIBER OPTICS TRANSMITTER INTEGRATED CIRCUIT DEVELOPMENT

Honeywell Inc.
Systems and Research Center
Minneapolis, Minnesota 55413

JULY 1978

Final Report June 1976 - December 1977

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REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: AFAL-TR-78-107	2. GOVT ACCESSION NO. / 3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle): FIBER OPTICS TRANSMITTER INTEGRATED CIRCUIT DEVELOPMENT	5. TYPE OF REPORT & PERIOD COVERED: Final Report, June 1976 to December 1977
	6. PERFORMING ORG. REPORT NUMBER: F0470-FR
7. AUTHOR(s): Ben R. Elmer	8. CONTRACT OR GRANT NUMBER(s): F-33615-76-C-1280
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Honeywell Systems and Research Center, 2600 Ridgway Parkway, Minneapolis, MN 55413	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 6096-01-76
11. CONTROLLING OFFICE NAME AND ADDRESS: Air Force Avionics Laboratory (DHE), Wright-Patterson Air Force Base, OH 45433	12. REPORT DATE: July 1978
	13. NUMBER OF PAGES: 118
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): 130p.	15. SECURITY CLASS. (of this report): Unclassified
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Fiber optics

Integrated Circuit

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report describes the development of the Fiber Optic Transmitter Integrated Circuit (FOTIC) from synthesis through analysis, layout, processing, packaging, and testing the 1050 parts that were delivered. Detailed test, burn-in, and qualification plans are also included. One of the highlights of this report is an Application Information section, written to inform users of the characteristics of the device that are not apparent from reading the specification.

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PREFACE

This final technical report on the Fiber Optics Transmitter Integrated Circuit (FOTIC) Development program was submitted by Honeywell Inc., Systems and Research Center, 2600 Ridgway Parkway, Minneapolis, Minnesota 55413, under Contract F33615-76-C-1280 for the U. S. Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio 45433. The AFAL Contract Monitor was Gary Gaugler. The Principal Investigator was Ben R. Elmer; Marvin Geske, Dave Fulkerson, and Greg Schmitz were the other major Honeywell contributors. The author wishes to acknowledge the significant contribution of Dr. J. Robert Biard of Spectronics. Dr. Biard defined the concept and major functions required, and contributed many hours of analysis and refinement. Further, the author wishes to acknowledge the significant contribution of Marvin Geske of Honeywell's Solid State Electronics Center for the detailed design and analysis of the circuit. This report has been reviewed. It is approved for public release; distribution unlimited.

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SECTION I
INTRODUCTION, SUMMARY, AND RECOMMENDATIONS

INTRODUCTION AND SUMMARY

This document constitutes the final technical report of a development program to design, fabricate, test, and deliver approximately 1000 monolithic Fiber Optic Transmitter Integrated Circuits (FOTIC). The FOTICs each contain all functions necessary to convert an electrical signal into a constant-current drive for a light-emitting diode (LED). Two components, the LED and the FOTIC, are all that is required to convert a digital transistor-transistor logic (TTL) signal in the range dc to 10M bits/s into a light signal suitable for propagation through a fiber optic waveguide or, with a suitable lens system, through space.

When properly packaged, these two components will constitute a general-purpose transmitter module for use in many military applications requiring highly reliable, low-cost, medium-performance characteristics.

In addition to describing, in detail, the FOTIC function and design, this report also contains complete test, burn-in, and qualification plans.

RECOMMENDATIONS

There are three major areas that can be addressed to improve the FOTIC with minimum risk.

- Packaging
- Yield improvement
- Increase applications.

Packaging

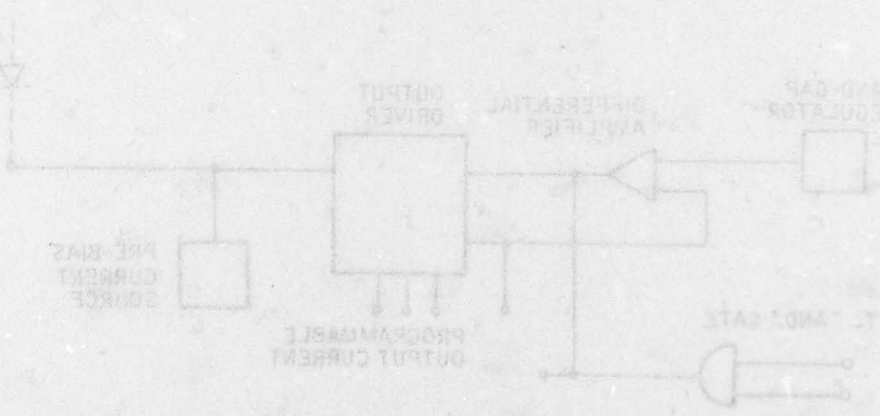
The TO-99 package is a very inexpensive, small, reliable, mature semiconductor package. However, its main disadvantage is its high thermal impedance (35 to 50°C/W). As pointed out in this report, a "good" heat sink is required for this package, even at very low output drive currents. A more reasonable packaging approach is to put the FOTIC in a leadless chip carrier (LCC). The LCC is really a miniature 14-pin DIP package that has equivalently low thermal impedance (10 to 15°C/W) and much shorter lead lengths. The cost of the LCC is less than a 14-pin DIP and can be mounted on a printed-circuit board or a hybrid substrate. Characterization of the FOTIC in this type package should reveal improved performance.

Yield Improvement

One of the functions of the FOTIC is to provide a pre-bias current of 1 to 50 μA. This report describes this function as being required by "some" LEDs to improve their rise time. This function can easily be performed by connecting an external 100-KΩ resistor from the output transistor collector to ground rather than putting this very large resistor "on chip." There probably would be a slight yield improvement if this function were removed from the chip and implemented externally for those cases when it is needed.

Increase Applications

One transmitter function not included on the FOTIC is the Manchester Encoder function. This encoder will be required for a number of applications and probably will be implemented in TTL externally. The circuitry required to implement this function is, at most, two flip-flops and two NAND gates which could be independently placed on the IC and wired in externally if used, or grounded out if not used. Two FOTIC versions could be available, so yield loss for the standard FOTIC (without the encoder) would not be affected.

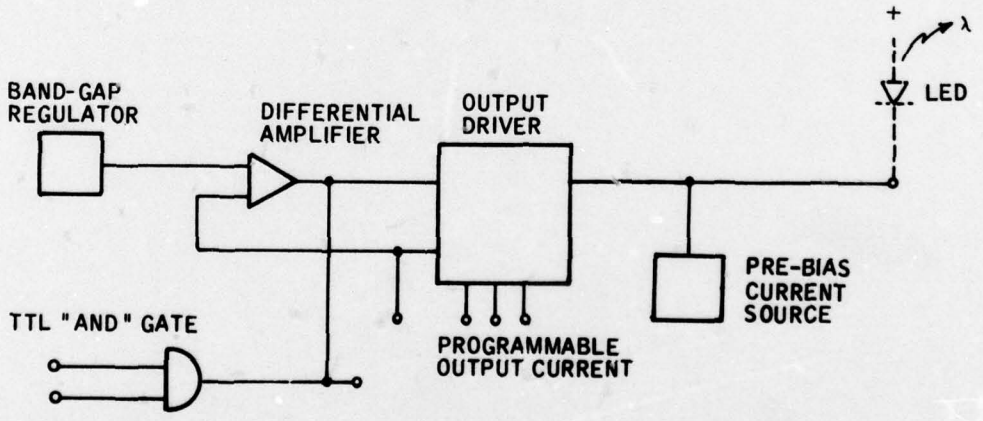


SECTION II

GENERAL FUNCTIONAL CAPABILITIES

Figure 1 is a block diagram and a listing of the salient characteristics of the FOTIC. The capabilities of the device to perform the required transmitter functions are discussed below.

The primary function of the FOTIC is to convert a digital TTL signal into the current drive for a light-emitting diode (LED). In some situations, this simple sounding function can be accomplished by a single transistor-transistor logic (TTL) power gate. For most applications however, the environment dictates more control over the LED current than can be obtained with a simple TTL gate.



CHARACTERISTICS:

1) CONSTANT OUTPUT CURRENT OVER -55 TO +125°C AND 5V ±10%.
2) PROGRAMMABLE OUTPUT CURRENT = 25 TO 150 mA.
3) DC TO 10 MBits/sec (8 ns DELAY, 5 ns τ_r, τ_f).
4) PRE-BIAS CURRENT FOR LED = 50 μA.
5) WORST-CASE POWER = 560 mW.

Figure 1. Fiber Optic Transmitter Integrated Circuit (FOTIC)

CONSTANT-CURRENT CAPABILITY

Studies performed on LEDs indicate that their first-order failure mechanism is a function of current density that produces excess power and overheats the LED. In the ambient temperature range of -55 to +125°C, the forward drive current of a LED can change by a factor of 2 to 4. This temperature environment leads to a requirement to control the LED forward drive current to a constant value.

The power supply variation of ±10 percent on a 5V supply leads to a 1V change which can produce a 20 percent change in LED drive current. A constant-current drive source can eliminate the power supply change as a factor in LED failures.

The constant-current capability provided by the FOTIC is a result of the special functions incorporated in its design. The band-gap regulator supplies a reference voltage to the differential amplifier which controls the output transistor to maintain whichever output current value is set by the programmable output resistors. This programmed output current is held constant over the aforementioned temperature and voltage range.

PROGRAMMABLE OUTPUT CURRENT CAPABILITY

There are a variety of LEDs that have different purposes. These various LEDs require different drive currents in the range of 25 to 150 mA. To avoid the necessity of designing various transmitters to provide this variety of drive currents, the FOTIC was designed to provide these various currents, each value being constant over the previously specified temperature and voltage range.

There are three specially-designed resistors that can be tied to ground either singly or in combinations to limit the output current to values between 25 and 150 mA in 25-mA increments.

INPUT GATING

The two inputs to the FOTIC are equivalent to standard 5400-type TTL inputs and they are interchangeable. One input is intended to be used as an enable for the other input so that many FOTICs may be multiplexed.

Use of Schottky diodes to prevent saturation enhances the speed of the TTL gate. The gate performs the AND function. Both inputs must be high (TTL "1") to turn ON the output transistor which in turn forces drive current through the LED that produces the light output. Either input being low (TTL "0") turns the output transistor OFF and also the LED.

PRE-BIAS CURRENT

Another capability of the FOTIC is the pre-bias current source. This current source ensures that when the output transistor is OFF, there is a small current pulled through the LED to keep it just below the turn-on point. This small pre-bias current enhances the turn-on speed of some LEDs.

SECTION III
APPLICATION INFORMATION

The FOTIC was delivered in three configurations: unpackaged chips, 14-pin ceramic DIPs, and 8-pin TO-99 cans. The unpackaged chips can be used on hybrid substrates or put in leadless carriers. They were d-c tested and visually inspected only. The DIPs and TO-99s were fully tested as described in Section VI under "FOTIC Test Plan."

DEVICE SPECIFICATION

The device specification has two parts, Electrical Characteristics and Environmental Conditions.

Electrical Characteristics

The performance characteristics shall apply over the operating temperature range of Table 1 and supply voltage V_{cc} ± 10 percent (-55°C to +125°C, +5V ± 10 percent). The IC shall operate as shown in Figure 2 and meet the d-c and a-c performance characteristics described next.

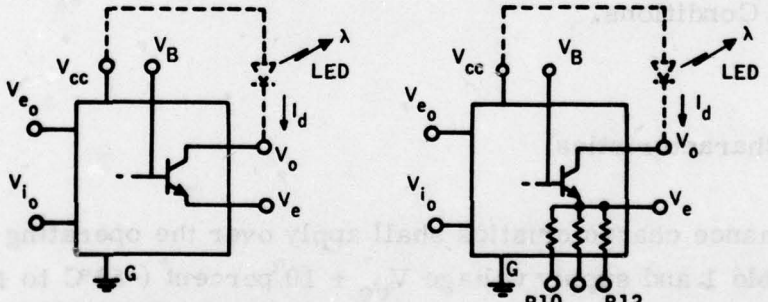
D-C Performance Characteristics

Maximum Ratings--The maximum ratings are specified in Table 1.

Supply Voltage and Current--The IC supply voltages shall be ground and +5V ± 10 percent, and the supply current shall not exceed the maximum output current (I_{DH}) plus 25 mA or 200 mA total, whichever is smaller.

TABLE 1. MAXIMUM RATINGS

Parameter	Value	Units
Supply voltage, V_{cc}:		
Operating	4.5 to 5.5	V
Non-operating	7.0	V
Input voltage (either input)	5.5	V
Supply current, I_{cc}	200	mA
Temperature, ambient (T_A):		
Operating	-55 to +125	°C
Nonoperating	-65 to +150	°C
Temperature, junction (T_J)	+150	°C
Power dissipation, P_D	875	mW
Lead temperature (soldering 10 sec)	250	°C



CONFIGURATION 1 (SEE NOTE)
(8-PIN TO-99)

CONFIGURATION 2
(14-PIN DIP)

V_{e_o} = OUTPUT ENABLE
V_{i_o} = TTL SIGNAL INPUT
V_{cc} = SUPPLY VOLTAGE
G = SUPPLY REFERENCE
V_o = OUTPUT VOLTAGE
I_d = OUTPUT CURRENT
V_e = EMITTER OF OUTPUT TRANSISTOR
V_B = BASE OF OUTPUT TRANSISTOR (FOR TESTING)
R10, R11, R12 = INTERNAL CURRENT-SETTING RESISTORS
NOTE: THIS CONFIGURATION REQUIRES A HEAT SINK (SEE SECTION ON POWER DISSIPATION).

Figure 2. Packaging Configurations

Input Characteristics--The input current and voltage levels shall be TTL compatible as specified in Table 2. Each input shall appear to be one standard 5400 series TTL input load.

TABLE 2. INPUT CHARACTERISTICS

Parameter	Test Condition	Min.	Typical	Max.	Unit
High-level input voltage, V_{IH}	---	2.0	2.4	---	V
Low-level input voltage, V_{IL}	---	---	0.4	0.8	V
Input clamp voltage, V_I	V_{cc} = 4.5V	---	-1.2	-1.5	V
Input current at maximum input voltage, I_I	V_{cc} = 5.5V, V_I = 5.5V	---	0.001	1	mA
High-level input current, I_{IH}	V_{cc} = 5.5V, V_I = 2.4V	---	1.0	40	μA
Low-level input current, I_{IL}	V_{cc} = 5.5V, V_I = 0.4V	---	-1.2	-1.6	mA

Output Characteristics--The output current from the IC shall be a current dependent on the input logic level, in accordance with Table 3. The output shall provide a controlled current (I_d) to the light-emitting diode (LED) load, selectable over a range from 25 to 150 mA in 25-mA increments.

A-C Switching Characteristics--The a-c switching characteristics from the input voltage to the output current shall be in accordance with Table 4 and Figure 3. The data rate of the IC shall be between dc and 10M bits/s (Manchester).

Environmental Conditions

The FOTIC shall be processed to meet MIL-STD-883B testing for Class B parts.

TABLE 3. OUTPUT CHARACTERISTICS

Parameter	Test Condition	Min.	Max.	Unit
High-level output current	V_{cc} = 5.5V, V_I = 2.4V	---	I_d[a] + 10%	mA
I_{DH} Configuration 1 (see Figure 2)	V_{cc} = 4.5V, V_I = 2.4V	I_d[a] - 10%	---	mA
High-level output current	V_{cc} = 5.5V, V_I = 2.4V	---	I_d[a] + 20%	mA
I_{dH} Configuration 2 (see Figure 2)	V_{cc} = 4.5V, V_I = 2.4V	I_d[a] - 20%	---	mA
Low-level output current, I_{dL}	V_{cc} = 5V, V_I = 0.4V	1	50	µA

[a] I_d is settable over a range from 25 to 150 mA in 25-mA steps.

TABLE 4. SWITCHING CHARACTERISTICS

Parameter	Min.	Typical	Max.	Units
Input transition time low-to-high, $T_{I_{LH}}$	4	---	6	ns
Input transition time high-to-low, $T_{I_{HL}}$	4	---	6	ns
Delay time low-to-high, $T_{D_{LH}}$	4	8	15	ns
Delay time high-to-low, $T_{D_{HL}}$	2	6	15	ns
Output transition time low-to-high, $T_{O_{LH}}$	4	6	7	ns
Output transition time high-to-low, $T_{O_{HL}}$	2	4	10	ns
Input pulse width T_1	40	---	---	ns
Output pulse width, T_2	T_1 - 5	T_1 - 2	T_1 + 5	ns

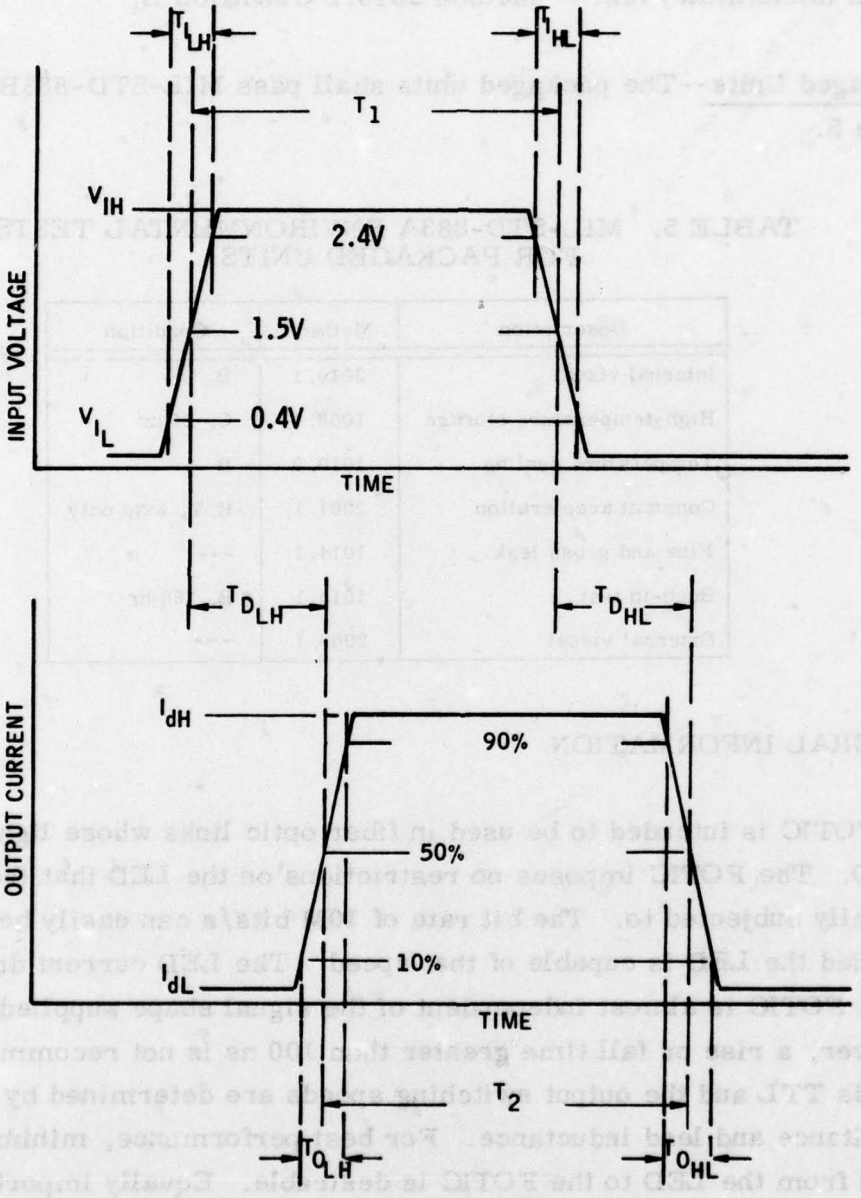


Figure 3. Input/Output Waveform Characteristics

Unpackaged Chips--The unpackaged chips shall pass MIL-STD-883B internal visual (monolithic) test -- Method 2010.2 Condition B.

Packaged Units--The packaged units shall pass MIL-STD-883B as shown in Table 5.,

TABLE 5. MIL-STD-883A ENVIRONMENTAL TESTS FOR PACKAGED UNITS

Description	Method	Condition
Internal visual	2010.1	B
High-temperature storage	1008.1	C, 24 hr
Temperature cycling	1010.0	B
Constant acceleration	2001.1	E, Y, axis only
Fine and gross leak	1014.1	---
Burn-in test	1015.1	B, 168 hr
External visual	2009.1	---

GENERAL INFORMATION

The FOTIC is intended to be used in fiber optic links whose light source is a LED. The FOTIC imposes no restrictions on the LED that the LED is not normally subjected to. The bit rate of 10M bits/s can easily be obtained provided the LED is capable of that speed. The LED current drive provided by the FOTIC is almost independent of the signal shape supplied to its input. However, a rise or fall time greater than 100 ns is not recommended. The input is TTL and the output switching speeds are determined by the LED capacitance and lead inductance. For best performance, minimum lead length from the LED to the FOTIC is desirable. Equally important, the ground connections for the on-chip resistors should be as close to the FOTIC ground pin as practical.

PIN CONNECTION INFORMATION

Figure 4 shows the pin connection diagrams for both package types. The pins labeled NC indicate that no internal connection is made to that pin, so it can be used for a tie point or ground.

POWER SUPPLY FILTERING

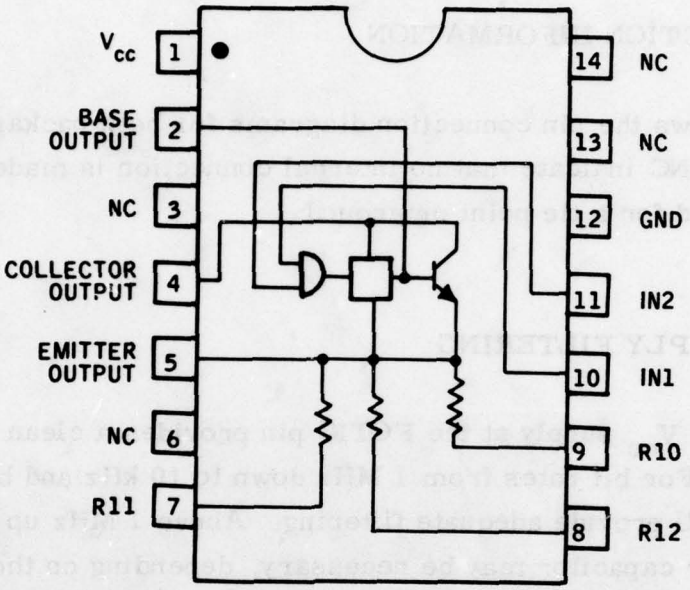
Filtering the V_{cc} supply at the FOTIC pin provides a clean output current waveform. For bit rates from 1 MHz down to 10 kHz and below, a 4.7-μF capacitor will provide adequate filtering. Above 1 MHz up to 10 MHz, a 0.1-μF filter capacitor may be necessary, depending on the supply itself. Since most of the FOTIC is TTL circuitry, ground, interconnection, and filtering techniques established for TTL systems will ensure proper performance.

OUTPUT CURRENT OBSERVATION METHOD

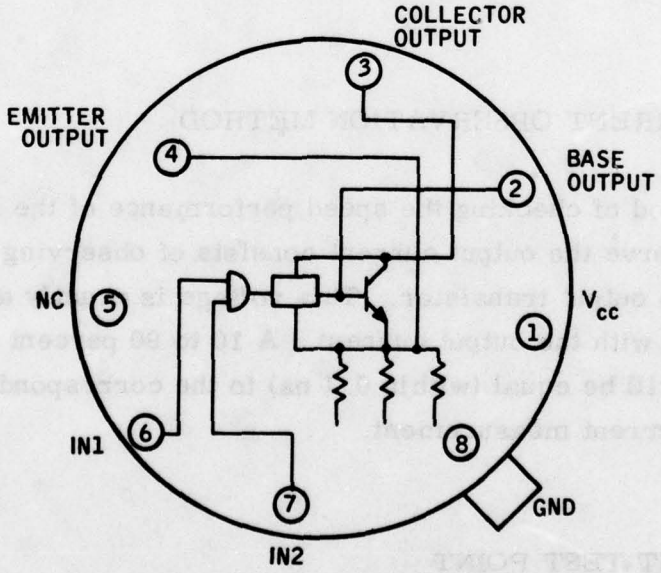
An easy method of checking the speed performance of the FOTIC without having to observe the output current consists of observing the voltage on the emitter of the output transistor. This voltage is exactly analogous in amplitude and time with the output current. A 10 to 90 percent measurement of this voltage will be equal (within 0.1 ns) to the corresponding 10 to 90 percent output current measurement.

BASE OUTPUT TEST POINT

The base output (pin 2 of 14-pin DIP and TO-99) can be used to monitor the switching state of the output transistor or as a test point for d-c



a) 14-PIN CERAMIC DIP



b) 8-PIN TO-99

Figure 4. Pin-Connection Diagrams for the 14-Pin Ceramic DIP and 8-Pin TO-99 Packaging Configurations

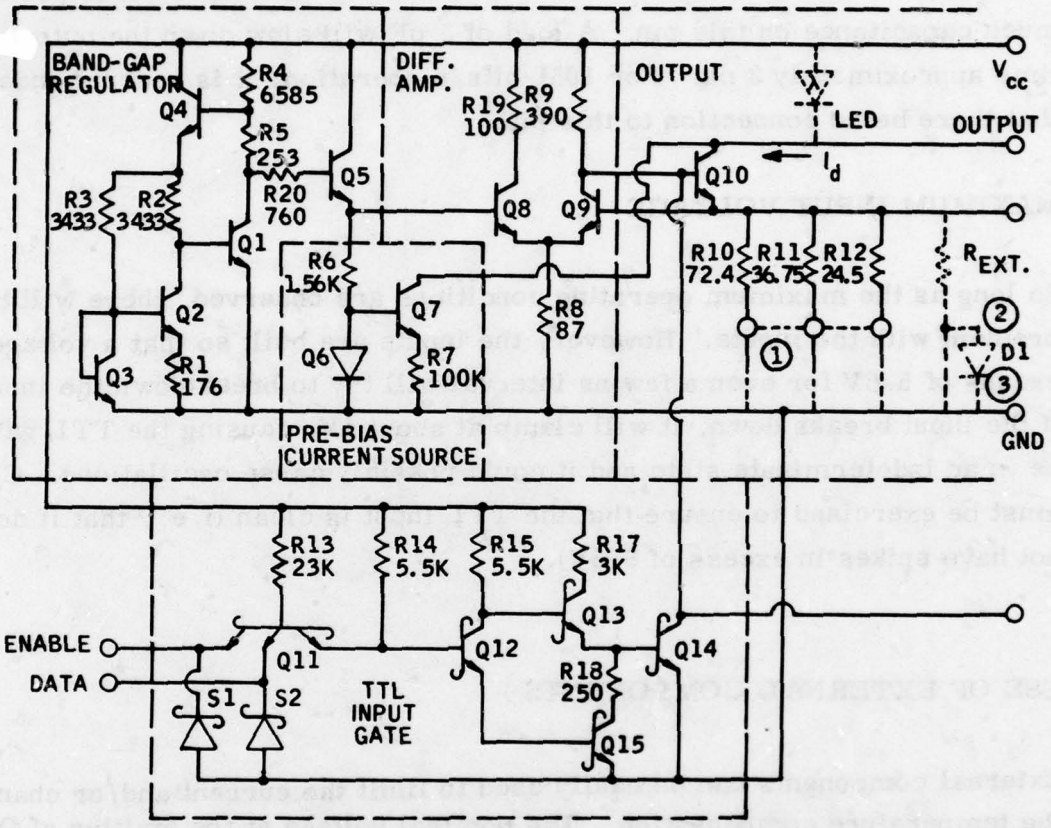
measurements on the output transistor. The TTL gate normally drives this base output between 0.4 and 2.5V. Care must be exercised not to put too much capacitance on this pin. A load of 5 pF will slow down the output rise time approximately 2 ns. For 10M-bits/s operation, it is recommended that there be no connection to this pin.

MAXIMUM INPUT VOLTAGE

So long as the maximum operating conditions are observed, there will be no problem with the inputs. However, the inputs are built so that a voltage in excess of 5.5V for even a few ns interval will try to break down the input. If the input breaks down, it will clamp at about 1V, causing the TTL gate to be in an indeterminate state and it could possibly cause oscillations. Care must be exercised to ensure that the TTL input is clean (i.e., that it does not have spikes in excess of 5.5V).

USE OF EXTERNAL COMPONENTS

External components can be easily used to limit the current and/or change the temperature compensation. The nominal voltage at the emitter of Q10 can be measured. Knowing that it changes with temperature at a +0.12%/°C rate, combinations of resistors and diodes similar to that shown in Figure 5 can be used to offset the LED temperature coefficient to produce a more constant light output at the expense of reduced LED life. This method of controlling LED light output over temperature is not recommended, but is available on the FOTIC.



NOTES:

1) COMBINATIONS OF R10-R12 TIED TO GND PRODUCE CONSTANT (0%/°C) OUTPUT I:
   a) R10 ONLY → 25 mA
   b) R11 ONLY → 50 mA
   c) R12 ONLY → 75 mA
   d) R10 + R12 → 100 mA
   e) R11 + R12 → 125 mA
   f) R10 + R11 + R12 → 150 mA
2) 0%/°C $R_{EXT.}$ TIED TO GND PRODUCES +0.12%/°C OUTPUT I.
3) 0%/°C $R_{EXT.}$ TIED TO D1 TO GND PRODUCES +0.36%/°C OUTPUT I.
4) ALL RESISTANCES IN OHMS.

Figure 5. FOTIC Schematic Diagram with External Compensation

DEVICE POWER CALCULATION

The power dissipated by the FOTIC can be separated into two major parts. There is a fixed power, independent of the LED current, I_{LED}, and a variable power directly dependent on I_{LED}. Methods of calculating these powers are presented below.

Fixed Power

The fixed power can be calculated by using the worst-case currents drawn by the chip in its two states. When output transistor Q10 is OFF, the FOTIC current, I_{OFF}, excluding I_{LED}, is 36.5 mA maximum at 125°C ambient.[1] When Q10 is ON, the FOTIC current I_{ON}, excluding I_{LED}, is 21.5 mA maximum at 125°C ambient. However, the specification requires that the devices be tested to ensure that the total current including I_{LED} is ≤ 200 mA. The "worst-case" method of calculating power, then, is to assume the highest I_{LED} and then subtract that from the 200 mA. The highest I_{LED} is 180 mA, so the highest I_{ON} is 20 mA. The I_{OFF} will be reduced by the same percentage as I_{ON}. Therefore, I_{OFF} = 34 mA. For a 50 percent duty cycle, the fixed power, P_F, is given by:

$$P_F = (V_{cc_{max}}) (I_{ON} + I_{OFF}) (50\%)$$

$$= (5.5) (34 + 20) (0.5) = 148.5 \text{ mW}$$

For "worst-case" calculations, the fixed power for I_{LED} < 150 mA nominal has no limitations on I_{ON} or I_{OFF}. Therefore, to calculate P_F for I_{LED} < 150 mA, use the "worst-case" I_{ON} and I_{OFF} values (see Table 6).

---

[1] The FOTIC current is higher than 36.5 mA at -55°C, but power dissipation is "worst-case" at highest temperature, 125°C.

TABLE 6. FOTIC POWER DISSIPATION

Parameter	Current Range						Units
Nominal LED current, I_{LED}	25.0	50.0	75.0	100.0	125.0	150.0	mA
On-chip resistor tied to ground	R10	R11	R12	R10 and R12	R11 and R12	R10, R11, and R12	---
External resistor value	73.12	36.45	24.25	18.15	14.50	12.06	Ω
Fixed power, P_F [a]	159.5	159.5	159.5	159.5	159.5	148.5	mW
Resistor power, P_R [b]	26.25	52.5	78.75	105.0	131.25	157.5	mW
Q10 power, P_Q [c]	36.75	73.5	110.25	47.0	183.75	220.5	mW
14-pin DIP FOTIC total power, P_{T14}	222.5	285.5	348.5	411.5	474.5	526.5	mW
8-pin TO-99 FOTIC total power, P_{T8}	196.25	233.0	269.75	306.5	343.25	369.0	mW

[a] Assumes 50 percent duty cycle.

[b] Assumes V_{EQ10} *constant* at 1.75V and +20 percent I_{LED} and Note a.

[c] Assumes 1.3V drop across LED and Note b.

Variable Power

The variable power can be calculated by breaking it into two parts. The first part is that power dissipated by the current-limiting resistors. These resistors are either on-chip (R10, R11, R12, in Figure 5) or are external and do not contribute to the FOTIC power. The other part of the variable power is the output transistor power.

On-Chip Resistor Power--To calculate the on-chip resistor power, the voltage at the emitter of Q10, V_{EQ10}, must be known. Assuming that V_{EQ10}, is relatively constant and independent of the output current, I_{LED}, a worst-case value of 1.75V can be used. [2]

[2] V_{EQ10} does vary with process parameters ±15% and with temperature +0.12%/°C and is nominally at 1.86V at 25°C. At 125°C, it is 2V nominally, 1.75V minimum (worst case for power with external resistors).

The worst-case current through the LED, Q10, and the resistors must also be known to calculate their power. The LED current is variable from a nominal value of 25 mA to 150 mA in 25-mA steps. Processing parameters will vary these nominal currents by ±10 percent in Q10 and the on-chip resistors add ±10 percent to the actual LED current. When using the on-chip resistors, the worst-case I_{LED} is +20 percent above nominal. If an external resistor is used, its tolerance and temperature coefficient must be added to the ±10 percent variation of Q10 current. The on-chip resistor power, P_R, for the 150-mA step and 50 percent duty cycle is:

$$P_R = (V_{EQ10})\,(I_{LED})\,(50\%) = (1.75)\,(180)\,(0.5) = 157.5 \text{ mW}$$

Output Transistor Power--The second part of the variable power is the power dissipated by output transistor Q10. A worst-case forward drop across the LED, V_{LED}, at 125°C will be assumed to be 1.3V. With this assumption, a V_{EQ10} = 1.75V plus a 50 percent duty cycle, the power dissipated in Q10, P_Q, for the 150-mA step is:

$$P_Q = (V_{cc_{max}} - V_{LED} - V_{EQ10})\,(I_{LED})\,(50\%)$$

$$= (5.5 - 1.3 - 1.75)\,(180)\,(0.5) = 220.5 \text{ mW}$$

Total FOTIC Power--The total FOTIC power can now be determined. For the 14-pin DIP package using the on-chip resistors, the total power, P_{T14}, for the 150-mA step and 50 percent duty cycle is:

$$P_{T14} = P_F + P_R + P_Q = 526.5 \text{ mW}$$

For the 8-pin TO-99 package using an external resistor whose worst-case value is -10 percent below nominal, the total power, P_{T8}, for the 150-mA step and 50 percent duty cycle is:

$$P_{T8} = P_F + P_Q = 369 \text{ mW}$$

Various powers for other current steps are tabulated in Table 6.

Thermal Resistance Considerations

The thermal resistance from junction to ambient, θ_{JA}, of the FOTIC packages must be such that with a 125°C ambient, T_A, the maximum junction temperature, T_j, of the chip is 150°C.

FOTIC T_j in 14-Pin DIP--For the 14-pin DIP soldered into a printed-circuit board with good solder fillets on the package pins and the ceramic package body resting on the copper-clad board surface, its θ_{JA} is 50°C/W.[3]

Using this value for θ_{JA}, the FOTIC junction temperature can be determined by using the total power listed in Table 6 and this equation:

$$T_j = (P_T)(\theta_{JA}) + T_A$$

Thus, for the 150-mA step in the 14-pin DIP, $T_j = (0.5265)(50) + 125 = 151$°C and no heat sink is required.

[3] Buchanan, R.C. and Reeber, M.D., "Thermal Consideration in the Design of Hybrid Microelectronic Packages," Solid State Technology, February 1973, pages 39 to 43.

FOTIC T_j in 8-Pin TO-99--For the 8-pin TO-99 package similarily mounted, its θ_{JA} is 143°C/W.[4] For the 8-pin TO-99 25-mA step with external resistors,

$$T_j = (0.19625)(143) + 125 = 153°C$$

For $I_{LED} > 25$ mA, a heat sink will be required. Assuming a heat sink compound is used to exclude air between the TO-99 case and the heat sink, the equation is modified to:

$$T_j = P_T(\theta_{JC} + \theta_{SA}) + T_A$$

where θ_{JC} is junction-to-case thermal resistance, about 35°C/W, and θ_{SA} is the heat sink thermal resistance. So, to determine the thermal resistance of the heat sink, solve the above equation for θ_{SA}. Using the 150-mA step P_{T8} from Table 6.

$$\theta_{SA} = \left(\frac{T_j - T_A}{P_T}\right) - \theta_{JC} = \left(\frac{25}{0.369}\right) - 35 = 33°C/W$$

This low value for θ_{SA} indicates a very good heat sink is required to drive a 150-mA LED current under worst-case 50 percent duty-cycle conditions.

The above values for θ were calculated with some assumptions that may not be valid. It is recommended that the user actually make thermal measurements on the TO-99 package mounted as he intends to use it, to make sure the T_j is not too high.

[4] "Thermal Management of Integrated Circuits," prepared by the staff members of the Semiconductor Products Division of Motorola, Inc., in a booklet entitled "Emerging Technology."

SECTION IV
CIRCUIT DESCRIPTION

The circuit description consists of two major parts, the general circuit operation and the detailed design analysis. The general circuit operation description is intended to give the reader an understanding of how the circuit accomplishes its task without referring to actual voltage or current values. Once the general circuit operation is understood, the detailed design analysis description will be much easier to understand.

GENERAL CIRCUIT OPERATION

The FOTIC is a programmable constant-current source that is switched ON and OFF by a digital gate and is used to drive a LED. The circuit consists of a temperature-compensated voltage reference, based on a band-gap regulator, a buffer feedback amplifier stage that drives the output current source, on-chip programming resistors to set the current value, a pre-bias current source for LED turn-on enhancement, and a Schottky-clamped TTL AND gate to modulate the current source. (See Figure 6.)

Band Gap Regulator

The detailed design approach to synthesize a band-gap regulator is well documented.[5,6] Essentially, the most stable and predictable property of

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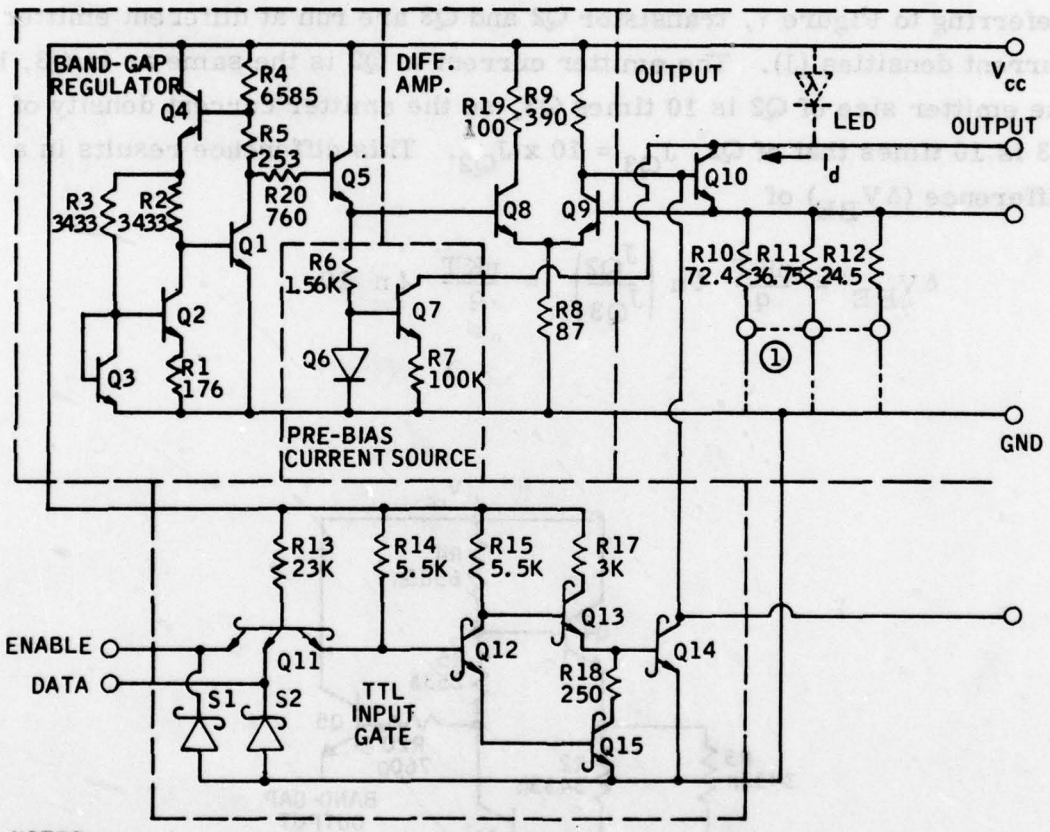
[5] Dobkin, Robert., "1.2-Volt Reference," National Semiconductor Application Note AN-56, National Semiconductor Corp., Santa Clara, 1971.

[6] Grebene, Alan B., Analog Integrated Circuit Design, Van Nostrand Reinhold, New York, 1972, pp 127-127.



NOTES:

1) COMBINATIONS OF R10-R12 TIED TO GND PRODUCE CONSTANT (0%/°C) OUTPUT I:
   a) R10 ONLY → 25 mA
   b) R11 ONLY → 50 mA
   c) R12 ONLY → 75 mA
   d) R10 + R12 → 100 mA
   e) R11 + R12 → 125 mA
   f) R10 + R11 + R12 → 150 mA
2) ALL RESISTANCES IN OHMS.

Figure 6. FOTIC Schematic Diagram

a silicon transistor, the base-emitter voltage (V_{BE}), is used as a reference to generate a voltage with a given temperature coefficient (TC) which becomes the output of the regulator.

Referring to Figure 7, transistor Q2 and Q3 are run at different emitter current densities (J). The emitter current in Q2 is the same as in Q3, but the emitter size of Q2 is 10 times Q3, so the emitter current density of Q3 is 10 times that of Q2, $J_{Q3} = 10 \times J_{Q2}$. This difference results in a V_{BE} difference (ΔV_{BE}) of

$$\Delta V_{BE} = \frac{nKT}{q} \ln \left(\frac{J_{Q2}}{J_{Q3}} \right) = \frac{nKT}{q} \ln 10$$

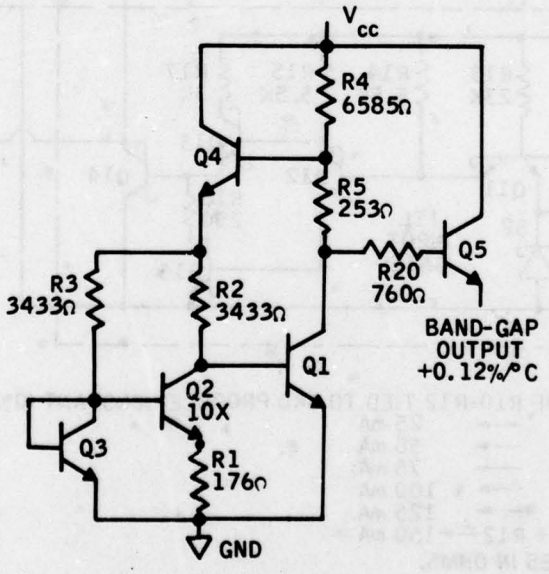


Figure 7. Band-Gap Regulator

where

T = °K

K = Boltzman's constant

q = Electronic charge

n = Process constant

which appears across R1 with a positive TC of $1/273°K \approx +0.36\%/°C$. For the Honeywell Advanced Bipolar Process I,[7] $\Delta V_{BE} \approx 59.7$ mV at 25°C. Neglecting Q1 and Q2 base currents, the current in R2 equals the current in R1, so the voltage across R2 is

$$V_{R2} = \Delta V_{BE} \left(\frac{R2}{R1}\right)$$

The band-gap voltage is the voltage at the emitter of Q4. This voltage is

$$V_{EQ4} = \Delta V_{BE} \left(\frac{R2}{R1}\right) + V_{BEQ1}$$

and its TC is the sum of the positive TC across R2 and the negative TC (-0.36% /°C) across V_{BEQ1}. By adjusting the R2/R1 ratio, the band-gap voltage can have zero TC or any value required. For the FOTIC, the TC was designed at +0.12% /°C. This value was picked to match the TC of the programmable resistors to obtain constant current over the temperature range.

The band-gap voltage, V_{EQ4}, is temperature compensated, but to get voltage compensation also, Q4, Q5, R4, and R5 were added. Rather than connecting the top of R2 and R3 to the supply directly, Q4 was added to partially decouple supply variations from V_{EQ4}. Q5 was added to give a

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[7] Appendix A contains a complete description of this advanced bipolar process

driving point equal to EQ4. The TC at EQ5 is equal to the TC at EQ4. The value of R5 was determined from computer simulations to give the smallest variation, over the temperature and voltage range, to the emitter of Q5. R20 was added later to squelch oscillations resulting from the emitter follower (Q5) driving a capacitive load. The emitter of Q5 has a +0.12%/°C TC and is essentially independent of supply variations.

Pre-Bias Current Source

The pre-bias current source consists of Q6 and Q7, R6 and R7 as shown in Figure 8. Without R7, it would look like any standard current source (i.e., whatever current flows through R6 and the diode-connected transistor, Q6, must also flow through Q7, independent of the load in Q7's collector). The current in Q7 is constant because the source of current for R6 and Q6 is from the emitter follower, Q5, whose emitter voltage varies +0.12%/°C. R6 was calculated so that the voltage across it also changed by +0.12%/°C; thus, the current through it is constant. R7 is added to ensure an output current of 2 μA minimum.

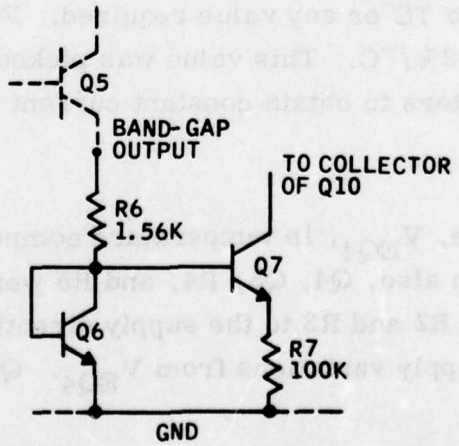


Figure 8. Pre-Bias Current Source

Differential Amplifier

When the FOTIC was being synthesized, the first design did not use the differential amplifier. The output transistor was driven directly from the band-gap output (EQ5). However, it was determined that the current drawn by the base of Q10 varied too much (from 125 μA to 3 mA) for Q5 to supply without upsetting the regulation. A buffer was required to separate the large output transistor base current variations from the band-gap output.

The differential amplifier shown in Figure 9 was added. It is driven from the emitter follower output of the band-gap regulator. It operates the same as any differential amplifier [i.e., given an input at one side's base (V_{BQ8}), it amplifies the difference between that base and its other base (V_{BQ9})]. Because the collecter of Q9, which is the differential amplifier output, is connected to the base of Q10, and the emitter of Q10 is connected back to the base of Q9, a feedback loop is formed. This feedback loops makes the differential amplifier try to maintain its bases equal to each other ($V_{BQ8} = V_{BQ9}$). Whether V_{BQ8} changes with temperature or V_{BQ9} tries to change with output current, both bases always try to be equal to each other. Thus, the emitter of Q10 (which is connected to the base of Q9) has the same voltage TC as the emitter of Q5, +0.12% /°C.

When $V_{BQ8} = V_{BQ9}$, the current through R9 equals the current through R19 and the current through R8 is equal to twice that through R9. Normally, the resistance value of R9 equals two times the value of R8, but for this design, R9 also acts as the pull-up resistor to turn Q10 ON. The base current of Q10 varies from 125 μA to 3 mA because of transistor beta variation and the programmable output current range of 25 to 150 mA.

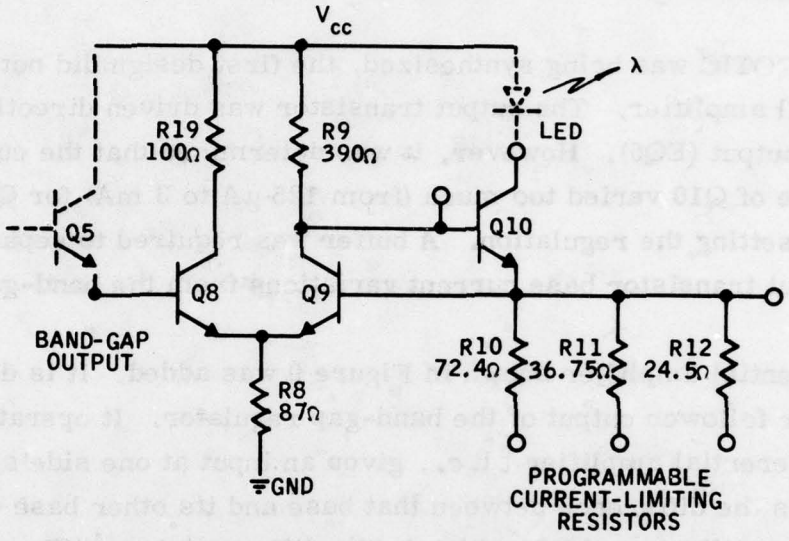


Figure 9. Differential Amplifier, Output Transistor, and Current-Limiting Resistors

When Q10 is OFF, the base of Q9 is pulled down almost to ground and the current in Q9 is essentially zero, while the full current limited by R8 goes through Q8. So, Q9 current is switched from zero to 1/2 I_{R8}, while Q8 current is switched from 1/2 I_{R8} to I_{R8}. In addition to these variations, the supply (V_{cc}) varies from 4.5 to 5.5V.

The value of R9 was originally picked to balance turn-ON and OFF time of Q10, but computer simulations trimmed that value to minimize the current imbalance in Q8 and Q9 with all the above variations taken into account. R19 was added later to suppress oscillations that could have occurred and frequently do occur with differential amplifiers built on high-performance processes, like the Honeywell Advanced Bipolar Process I.

On-Chip Programming Resistors

Again referring to Figure 9, the on-chip resistors (R10, R11, R12) used to limit the output current are made from emitter diffusion rather than base or collector diffusion because it has the most linear TC (+0.12%/°C) of all the available resistor diffusions. When any or all of the emitter diffused resistors (R10, R11, R12) are connected between ground and the emitter of Q10, the current through them is constant over the entire temperature range because both their value and the voltage across them vary at the same rate.

Power supply voltage variations have very little effect on the output current because the emitter voltage of Q10 is insensitive to them (it is a duplicate of the band-gap output) and the LED is in the collector of Q10, which means the voltage variation across it has very little effect on emitter current.

Thus, the constant output current of the FOTIC is a function of how well the band-gap output tracks temperature and voltage variations, plus it is a function of the difference between the differential amplifier bases that is controlled by the current imbalance in their emitters.

TTL Gate

The input of the TTL gate is the familiar multiple-emitter, Schottky-clamped transistor, Q11 (see Figure 10). Each input emitter is clamped to ground by a reverse-biased Schottky diode. The Schottky clamp prevents the input voltage from going negative more than the drop across it. It was made minimum size for the specified maximum current to minimize the input capacitance.

Q12 is the equivalent of the so called "phase splitter" in normal TTL gates. Its emitter drives Q16, which turns OFF the gate output transistor, Q14,

while its collector drives Q13, which turns Q14 ON. The drives to Q13 and Q15 were made equal so that Q14 would turn ON and OFF with the same speed. The values of resistors R13 through R17 were made as large as possible to minimize the power supply current drain, for minimum chip power. All transistors in the gate are Schottky clamped to prevent saturation which would severely limit their speed. The open collector gate output, Q14, and passive pull-up, R9, turns the output transistor Q10 OFF and ON.

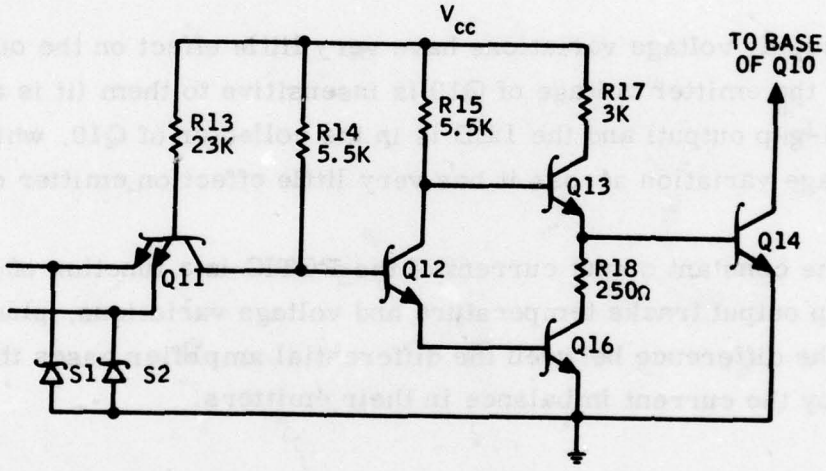


Figure 10. TTL "AND" Gate

DETAILED DESIGN ANALYSIS

A detailed design analysis was performed on the nominal parameter values picked during synthesis of the FOTIC circuit configuration. Some of the reasoning and equations developed to examine worst-case conditions and parameter values are presented in the following paragraphs. The FOTIC specification given in Section III was used as the input to the analysis and

the analysis results are measured to determine the predicted performance versus specification requirements. The results of this analysis were used to generate the information presented under "Test Plan" in Section VI.

Maximum Ratings

The maximum rating values listed in Section III, Table 1 are included in the specification to indicate the limits that the chip should be subjected to. The devices will not be damaged if exposed to these conditions, but if they are exceeded, the device may fail.

Maximum Supply Voltage--The FOTIC must withstand V_{cc} = 7.0V but not necessarily operate there. The maximum operating voltage is 5.5V. The process specifications which show that the device can easily meet these conditions are listed below:

Parameter	Nominal Value	Variation from Nominal
BV_{C-SUB}	35V	-15V
BV_{CBO}	20V	- 3V
BV_{CEO}	10V	- 3V

Maximum Supply Current--The maximum supply current $I_{cc_{max}}$ is given as 200 mA, including the largest value of I_{LED}. To calculate this current, the case with on-chip resistors will be used. The maximum deviation of I_{LED} has been calculated as 9 percent (see following paragraphs titled "Output Current Limited by On-Chip Resistors"). Assuming the on-chip resistor tolerance of 11 percent, these two deviations are added together (RSS) since they correlate.

RSS stands for root sum square which means each number is squared, then the squares are added together. Finally, the square root of the summed squares is taken to obtain the RSS value.

Thus:

$$\left[(0.11)^2 + (0.09)^2\right]^{1/2} = 14.2\%$$

The maximum I_{LED} then is

$$(150 \text{ mA})\ (114.2\%) = 171.3 \text{ mA}$$

From Table 15, $I_{cc} = 22.9$ mA.

Then,

$$I_{cc_{max}} = 171.3 + 22.9 = 194.2 \text{ mA}$$

Notice that the device is tested for $I_{cc_{max}} = 200$ mA at 150°C, T_j, and for the maximum $I_{LED} = 180$ mA (150 + 20 percent). It can happen that the operating current is less than 22.9 mA and I_{LED} has a +20 percent tolerance; thus, $I_{cc_{max}} \leq 200$ mA.

Maximum Junction Temperature--It will be assumed that the maximum safe operating junction temperature for reliable performance of silicon devices is +150°C. The design of the FOTIC has been carried out using this junction temperature rather than the maximum ambient temperature of +125°C.

Maximum Power Dissipation--The maximum power dissipation will occur with the on-chip resistor connected for the maximum I_{LED} condition and $V_{cc} = 5.5$V. The $I_{cc_{max}}$ was previously calculated as 194.2 mA, with the maximum $I_{LED} = 171.3$ mA. Assuming a minimum forward voltage drop across the LED of 1.3V, the maximum power dissipation is (194.2) (5.5) - (171.3) (1.3) = 845 mW which is less than the 875 mW maximum allowed. Another method for calculating this power uses the test limits. The maximum $I_{LED} = 180$ mA is tested at $I_{cc_{max}} = 200$ mA. The maximum power

would then be (200) (5.5) - (180) (1.3) = 866 mW, which also is less than the 875 mW maximum allowed.

Input Characteristics

Some of the input characteristics are not defined by the specification, but are standard TTL specifications that can be found in almost any handbook on TTL.

Input Clamp Voltage--The clamp diodes, S1 or S2, must clamp the input at -1.5V with 12 mA forward current through it. The Schottky diodes used to perform this function have nominal parameters that are derived in Section V, under "Layout Considerations." The parameters of interest are summarized in Table 7. They are the reverse saturation current per unit area, I_o, the resistance unit area, R_o, and the Schottky contact voltage, V_c.

TABLE 7. SCHOTTKY DIODE PARAMETERS

Parameter	Operating Temperature			Units
	-55°C	+25°C	+150°C	
I_o	1.2×10^{-19}	4×10^{-14}	1.2×10^{-9}	A/μ^2
V_c	0.020657	0.028237	0.040082	V
R_o	1.52×10^{4}	1.9×10^{4}	2.49×10^{4}	$\Omega\text{-}\mu^2$

With these unit values, and the Schottky area, A, defined, the following equations can be evaluated and the input clamp voltage (diode drop) at 12 mA forward current (I_{SH}) at each temperature can be determined:

R_{SH} = Schottky series resistance = R_o/A

I_S = Schottky saturation current = $I_o * A$

V_{clamp} = Total diode drop = $I_{SH} R_{SH} + V_C \ln (I_{SH}/I_S)$

The area for the Schottky diodes was chosen to ensure that the metallization covering it would carry 25 mA without any metal migration. The contact area chosen was 20 x 20 μ or 400 μ^2 The calculated results are given in Table 8.

TABLE 8. SCHOTTKY DIODE FORWARD VOLTAGE OVER TEMPERATURE RANGE

V_{clamp}	=	$I_{SH}R_{SH}$	+	V	Temperature
1.141V	=	0.456	+	0.685	- 55°C
1.147V	=	0.570	+	0.577	+ 25°C
1.156V	=	0.750	+	0.406	+150°C

Input Noise Margin--The noise margin is commonly referred to as the difference between the worst-case output level and the worst-case input level of a TTL gate. For FOTIC input, the worst-case levels are stated as 0.8V maximum input voltage and 2.0V minimum input voltage. Since there is no TTL output on the FOTIC which can be measured to meet the foregoing specification as normally spelled out in TTL handbooks, an equivalent I_{LED} was determined. For the maximum input of 0.8V, I_{LED} = 1 mA was measured with R10 grounded (refer to Figure 6). For the minimum input of 2.0V, I_{LED} = 130 mA was measured with R10, R11, and R12 grounded

(150 mA case). Computer simulations at all temperatures and voltages were run and verified the above conditions.

Input Current--There are three conditions of interest for designing the input current. First, the input current at the maximum input voltage (5.5V) is limited to 1 mA. Next, the "normal" operating input voltage (2.4V) has a maximum input current of 40 μA associated with it. Finally, the maximum input current with the low-level input voltage at 0.4V is -1.6 mA over the temperature range.

To accomplish the first two requirements, the initial design used standard TTL design procedures to kill the transistor inverse beta. The tied-back emitter had a K factor of 6[8] and I_b was calculated for the worst-case condition of one input at ground (0V) while the other input was maximum (5.5V). Again referring to Figure 10,

$$I_{B_{Q11}} = \frac{V_{cc} - V_{BE_{min}}}{R13_{min}} = \frac{5.5 - 0.7}{(23K)\ (0.8)} = 0.26\ mA$$

assuming -20 percent tolerance on R13. If the inverse beta of Q11 is 3 or less, the input current will be less than 1 mA. However, this design did not meet the requirements because Q11 had a very low reverse early voltage (the emitters act like collectors when the inputs are at voltages greater than 2V). This effect caused excessive current when the input voltage reached 4.2V.

The input stage was redesigned by putting a Schottky diode across the base-collector junction and removing the tied-back emitter. The Schottky ensures that the base-collector junction cannot turn ON, and thus the lateral NPN transistor made by the two emitters and the base cannot turn ON either.

[8] Fulkerson, D., "Direct-Coupled TTL; A New High-Performance LSI Gate Family," IEEE Journal of Solid State Circuits, Vol. SC-10, No. 2, April 1975.

Simulations showed that less than 10 μA flowed into the input at 5.5V. Thus, both input "high" conditions (2.4V and 5.5V) were well within the requirements. The disadvantage of the Schottky-clamped Q11 is the reduction in input threshold voltage at high temperatures.

The input current at the maximum low-level voltage (V_{in} = 0.4V) was determined as follows.

Assume:

a) ±20% absolute resistor tolerance

b) Temperature coefficient of resistors +0.2%/°C for T < 23°C

c) $I_{ES(T)} = I_{ES(23°C)} \left[e^{47.6\ (1\ -\ 296/T)}\right]$

d) $I_{ES(23°C)} = 1.18 \times 10^{-16}A$

e) I_{ES} absolute tolerance = -65%, +200%

f) Inverse beta ≤ 5

g) V_{CEQ11} at -55°C ≥ 0.3V

Then:

1) R13 is minimum at -55°C, so $R13_{min}$ = 23K (0.8) -0.002(78) (23) (0.8) = 15.53K

2) R14 is minimum at -55°C, so $R14_{min}$ = 5.5K (0.8) -0.002(78) (5.5K) (0.8) = 3714Ω

3) The input current is highest at -55°C, so to calculate it at that temperature, I_{ES} (-55°) and V_{BE} (-55°) must be calculated.

4) $I_{ES}(-55°C) = \left[I_{ES(23°C)} - I_{ES(23°C)}\ (0.65)\right]\left[e^{47.6\ (1\ -\ 296/218)}\right]$
$= 1.66 \times 10^{-24}A$

5) $V_{BE}(-55°C) = (0.026)\frac{218}{296}\ell n \frac{I_E}{I_{ES(-55°C)}} = 0.927V$ for I_E
$= 1.6$ mA

Then:

$$I_B = \frac{V_{cc} - V_{BE}(-55°C) - V_{in}}{R13_{min}} = \frac{5.5 - 0.927 - 0.4}{15.53K} = 269\ \mu A$$

and

$$I_{in} = \frac{V_{cc} - V_{CEQ11} - V_{in}}{R14_{min}} + I_B = \frac{5.5 - 0.3 - 0.4}{3714} + 269 = 1.56\ mA$$

which is less than the 1.6-mA requirement.

Output Characteristics

There is only one output, and its characteristics are defined by two states, OFF and ON. However, there are various levels of output current when the output is ON, so the analysis becomes quite involved. An additional complication is created by the requirements for two package types, a 14-pin DIP and an 8-pin TO-99. The TO-99 does not have enough pins to allow the on-chip programmable resistors to be used, so analysis for this case is also presented.

Output Current Limited by On-Chip Resistors--Ideally, the output current is constant. Practically, the parameters of the circuit vary with processing and with the actual design to produce a tolerance on this ideal constant current. For this design, there are three contributors to the tolerance on the output current (refer to Figure 6):

a) The input or reference for the differential amplifier has a variation caused by the non-ideal parameters of the band-gap regulator.

b) The differential amplifier itself has a "built-in" tolerance associated with its ability to maintain equal base voltages. The difference in the V_{BE}s of each transistor will introduce an offset that contributes to the overall non-ideal output current.

c) Finally, the design of the differential amplifier itself, with all the various factors contributing to the inbalance in the currents in Q8 and Q9, ensures a non-ideal output current.

To get some practical bounds on the band-gap regulator output variation, a sensitivity analysis was performed. Each major contributor to its error was varied one at a time, plus groups of contributors were varied together to get a column of variations that could be added together to give a total variation of the band-gap output. These variations exist at each temperature and supply voltage that the band gap-regulator is subjected to. Table 9 presents this sensitivity analysis for three values of power supply and three temperatures for each supply value. The numbers shown are the percent change in I_{LED} as a result of the parameter being changed by the indicated tolerance. The total change for each of these columns is obtained by calculating the RSS value.

The mismatch of Q8 and Q9 V_{BE}s is not greater than 4 mV. This error term is not a major source of error, but it must be considered. Its error value can be obtained by taking its change relative to the total change (minimum value) on the base of Q9. The minimum voltage change on Q9 is 1.8V, so the mismatch of Q8 and Q9 V_{BE}s contribute 0.004/1.8 = 0.2 percent.

TABLE 9. SENSITIVITY ANALYSIS OF BAND-GAP REGULATOR

Parameter Varied	Ideal Parameter Value	Tolerance Assumed (%)	Change in I_{LED} (%)								
			V_{cc} = 4.5V			V_{cc} = 5.0V			V_{cc} = 5.5V		
			-55°C	+25°C	+150°C	-55°C	+25°C	+150°C	-55%	+25°C	+150°C
I_S of Q1	1.38×10^{-16} A	100	-0.15	-0.19	-0.24	-0.15	-0.19	-0.24	-0.15	-0.19	-0.24
I_S of Q2	13.8×10^{-16} A	100	2.04	2.57	3.17	2.04	2.57	3 14	2.04	2.57	3.18
I_S of Q3	1.38×10^{-16} A	100	-1.98	-2.50	-3.09	-1.98	-2.50	-3.09	-1 98	-2.51	-3.10
I_S of Q4	1.38×10^{-16} A	100	-0.10	-0.13	-0.16	-0.11	-0.13	-0.16	-0.11	-0.13	-0.16
I_S of Q5	1.38×10^{-16} A	100	0.11	0.13	0.16	0.11	0.13	0.16	0.11	0.13	0.16
R1	176.5 Ω	20	-0.99	-1.23	-1 51	-0.99	-1.24	-1.52	-0 99	-1.25	-1.53
R2	3433 Ω	20	1.47	1.82	2.21	1.49	-1.83	2.23	1.50	1.84	2.24
R3	3433 Ω	20	-0.47	-0.57	-0.70	-0.47	-0.58	-0.70	-0.47	-0.58	-0.70
R4	6585 Ω	20	-0.01	-0.01	-0.02	0.00	0.00	-0 02	0.01	0.01	0.01
R5	190 Ω	20	-0.07	-0.05	-0.04	-0.08	-0.07	-0.05	-0.10	-0.08	-0.06
R6	1560 Ω	20	0.03	0.03	0.04	0.03	0.03	0.04	0.03	0.03	0.04
All resistors		20	-0.47	-0.52	-0.56	-0.48	-0.53	-0.57	-0.49	-0.54	-0.58
β and I_S	Note 1	Note 2	-1.49	-0.62	-1.15	-1.0	-0.77	-1.25	-0.53	-0.92	-1.34
RE of Q1	5.0 Ω	10	0.01	0.01	0.01	0.02	0.01	0.01	0.02	0.02	0.01
RE of Q2	0.5 Ω	10	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02
RE of Q3	5.0 Ω	10	0.16	0.17	0.17	0.16	0.17	0.17	0.16	0.16	0.17
RE of Q4	5.0 Ω	10	0.02	0 02	0.02	0.02	0.02	0.02	0.02	0.02	0.02
RE of Q5	5.0 Ω	10	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02	-0.02
RSS of all changes			3.74	4.33	5.39	3.56	4.36	5.40	3.48	4.37	5.46

Note 1. β = 80 and $I_S = 1.38 \times 10^{-16}$ A for minimum transistor.

Note 2. Correlation assumed between β and I_S. For β = 2x, I_S was assumed 0.35x; for β = 0.5x, I_S = 3x. Both cases were calculated but only the worst value is recorded above.

The nominal design values used in the differential amplifier create an error in the ideal output current value. Computer simulation of this circuit produced the actual nominal values obtained at different temperatures and voltages for the various output values shown in Table 10. The numbers shown in the "deviation from ideal" columns are percentage changes in I_{LED}.

TABLE 10. NOMINAL DESIGN VALUE OF I_{LED}

V_{cc} (V)	Ideal I_{LED} (mA)	Nominal Design Value I_{LED} (mA)			Deviation From Ideal (%)		
		-55°C	+25°C	+150°C	-55°C	+25°C	+150°C
4.5	25	25.22	25.37	24.67	0.88	1.48	1 32
	50	49.38	49.80	48.51	-1.24	-0.40	-0.98
	75	73.64	74.49	72.66	-1.81	-0.68	-3.12
	100	98.15	99.48	97.31	-1.35	-0.52	-2.69
	125	121.59	123.53	120.76	-2.73	-1.18	-3.39
	150	146.14	148.44	145.55	-2.57	-1.04	-2.97
5.0	25	25.53	25.60	24.89	2.12	2.40	-0.44
	50	49.95	50.25	48.95	-0.10	0.50	-2.10
	75	74.49	75.17	73.31	-0.68	0.23	-2.25
	100	99.30	100.40	98.21	-1.70	0.40	-1.79
	125	123.07	124.70	121.88	-1.54	-1.04	-2.50
	150	148.03	149.91	146.94	-1.31	0.06	-2.04
5.5	25	25.84	25.80	25.07	3.36	3.20	0.28
	50	50.50	50.63	49.28	1.00	1.26	1.44
	75	75.28	75.74	73.83	0.37	0.98	-1.56
	100	100.33	101.15	98.90	0.33	1.15	-1.10
	125	124.34	125.65	122.75	-0.53	0.52	-1.80
	150	149.59	151.07	148.00	-0.27	0.71	-1.33

These three error terms are relatively independent of each other and thus add directly rather than RSS. Table 11 condenses the data from Tables 9 and 10 by using the worst values for the given temperature and current level without regard to power supply voltage.

To meet the specification, these deviations must be less than ±10 percent, which they are. When the tolerance of the output resistor is added (RSS) to these values, the worst-case tolerance should be ≤ 20 percent.

TABLE 11. CALCULATED DEVIATION OF I_{LED}

Ideal I_{LED} (mA)	Calculated Deviation of I_{LED} (%)		
	-55°C	+25°C	+150°C
25	7.30	7.77	6.88
50	5.18	5.83	7.76
75	5.75	5.55	8.78
100	5.79	5.72	8.35
125	6.67	5.75	9.05[a]
150	6.51	5.61	8.63

[a]Maximum deviation.

Output Current Limited by External Resistor--For an external resistor with zero TC connected to the emitter of Q10, the output current varies with temperature +0.12%/°C. The tolerance on the output current without a resistor is ±10 percent. The external resistor temperature coefficient plus its tolerance must be known to calculate the value of output current for this condition.

A listing of the output current value for the nominal case at three temperatures is given in Table 12. The external resistor characteristics plus the ±10 percent tolerance must be added to these values.

TABLE 12. I_{LED} WITH EXTERNAL RESISTOR

Nominal I_{LED} When Used With an External Resistor(s)			Units
-55°C	+25°C	+150°C	
22.6	25	28.75	mA
45.2	50	57.5	mA
67.8	75	86.25	mA
90.4	100	115.0	mA
113.0	125	143.75	mA
135.6	150	172.5	mA

Power Supply Current Drain

The power supply current drain (I_{cc}) is of interest for both states of the output transistor. To evaluate the power supply current drain, computer simulation was again used along with some hand calculations. The six I_{cc} values of interest taken from the computer simulations are shown in Table 13.

TABLE 13. NOMINAL I_{cc}

Parameter	Operating Temperature			Units
	-55°C	+25°C	+150°C	
I_{cc} with Q10 ON	18.25	18.03	19.28	mA
I_{cc} with Q10 OFF	31.93	30.66	30.67	mA

Table 13 lists the nominal values at V_{cc} = 5.5V. To find the variations on these nominal values, a sensitivity analysis was performed. The transistor's beta, I_S, and r_b' were varied together. The tolerances on these parameters are shown in Table 14. The resistor values were changed by -20 percent to produce the highest current. The delta changes were added (RSS), since the parameters all correlate. Finally, the percent change from nominal current was calculated for the RSS value. This percentage was then used to determine the worst-case variation on the nominal value of supply current at the three temperatures at V_{cc} = 5.5V, as shown in Table 15.

TABLE 14. SENSITIVITY ANALYSIS FOR I_{cc}

Parameter	Sensitivity at 5V, 25°C, I_{cc} = 28.94 mA			Units
	Tolerance (%)	Total I_{cc}	ΔI_{cc}	
Beta	+100	---	---	---
I_S	+200	---	---	---
r_b'	+50	29.15	0.21	mA
High resistors	-20	29.91	0.97	mA
Low resistors	-20	34.31	5.37	mA
			RSS = 5.46	mA
			5.46/28.94 = 18.9	%

TABLE 15. WORST-CASE TOTAL I_{cc}

Parameter	Calculated Total I_{cc}			Units
	-55 C	+25 C	+150 C	
I_{cc} with Q10 ON	21.70	21.44	22.92	mA
I_{cc} with Q10 OFF	37.96	36.45	36.47	mA

Switching Characteristics

The switching characteristics were determined by computer simulation. Results are tabulated in Table 16 for nominal parameter values. Only the extreme conditions were simulated (i.e., V_{cc} = 4.5V at -55°C and V_{cc} = 5.5V at +150°C). The nominal case, V_{cc} = 5V at 25°C, was included for typical values. See Section III, Figure 3 for meaning of symbols.

TABLE 16. SWITCHING CHARACTERISTICS DERIVED FROM COMPUTER SIMULATIONS

Conditions	$T_{O_{HL}}$	$T_{O_{LH}}$	$T_{D_{HL}}$	$T_{D_{LH}}$	$T_{D_{HL}} - T_{D_{LH}}$	Units
Specification	10.0	7.0	15.0	15.0	5.0	ns
4.5V at -55°C	2.0	4.0	5.5	9.5	4.0	ns
5.0V at +25°C	2.0	3.0	5.0	5.5	0.5	ns
5.5V at +150°C	2.5	3.0	5.0	7.5	2.5	ns

SECTION V
DEVICE PARAMETERS

The initial synthesis of a circuit can be realized using estimated values for device parameters. However, before circuit simulation can be finalized and the layout completed, the device parameters must be derived for the specific size devices to be used.

This section gives examples of this device parameter derivation and summarizes the data obtained for the FOTIC.

Figure 11 is a detailed schematic of the FOTIC, including all its passive parasitic components that were derived.

TRANSISTOR PARAMETERS

There are nine different transistors out of a total of 15 used in the FOTIC. These nine are basically different sizes of two basic styles of transistor layout. Figure 12 shows the basic structure used for Q1 through Q10 (see Figure 11 for transistor numbering). This structure is characterized by the placement of the base in between the emitter and collector, termed EBC structure. Q1 and Q3 through Q7 also have double base stripes and feature a square emitter. Q2 has 10 square emitters each the size of Q1's but has a single base stripe. Q8 and Q9 have emitters five times the area of Q1 and have double base stripes. Q10's emitter has three equal emitters whose total area is 50 times that of Q1.

These features yield the following necessary characteristics:

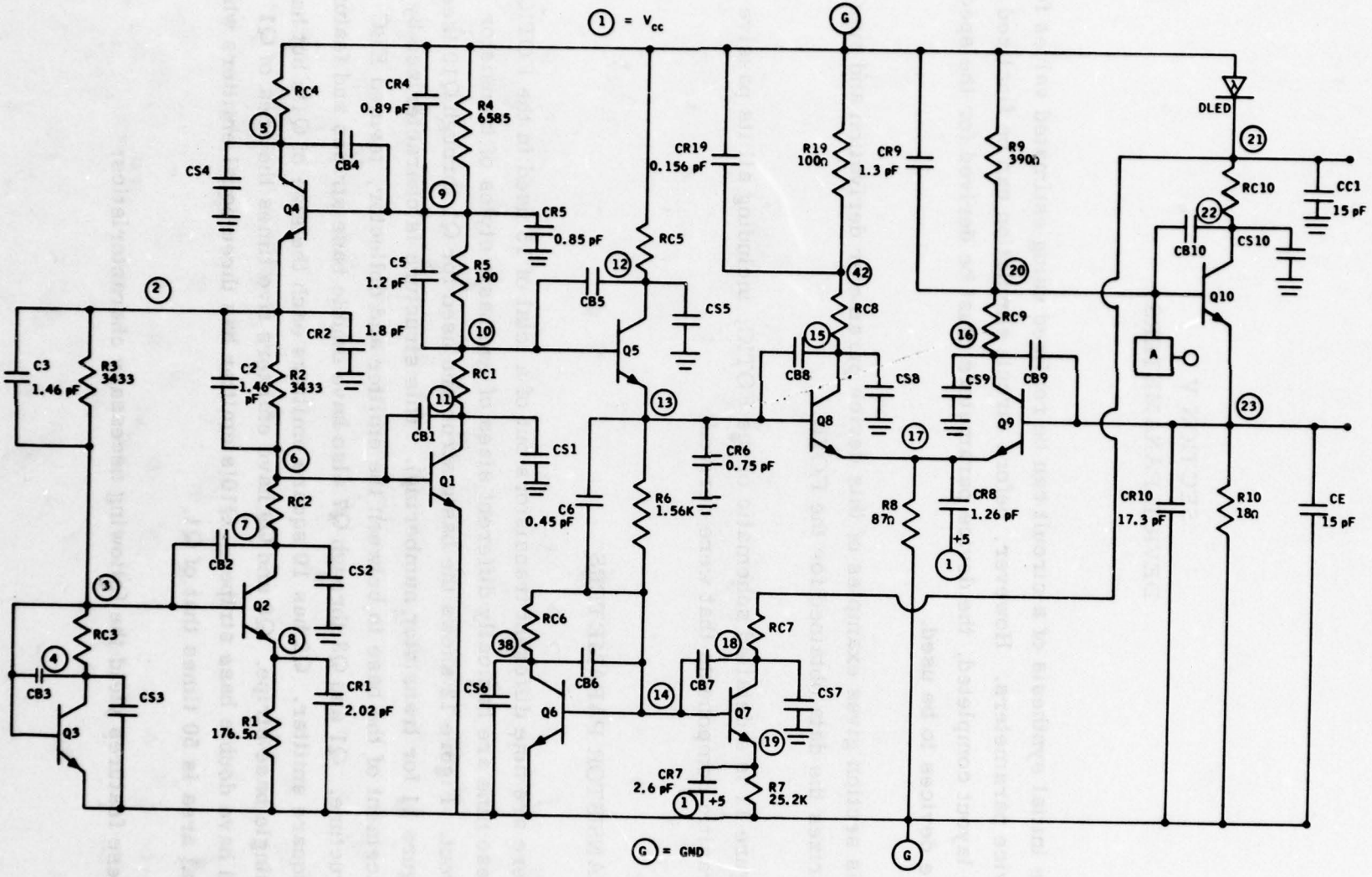


Figure 11. Circuit Diagram for Computer Simulation

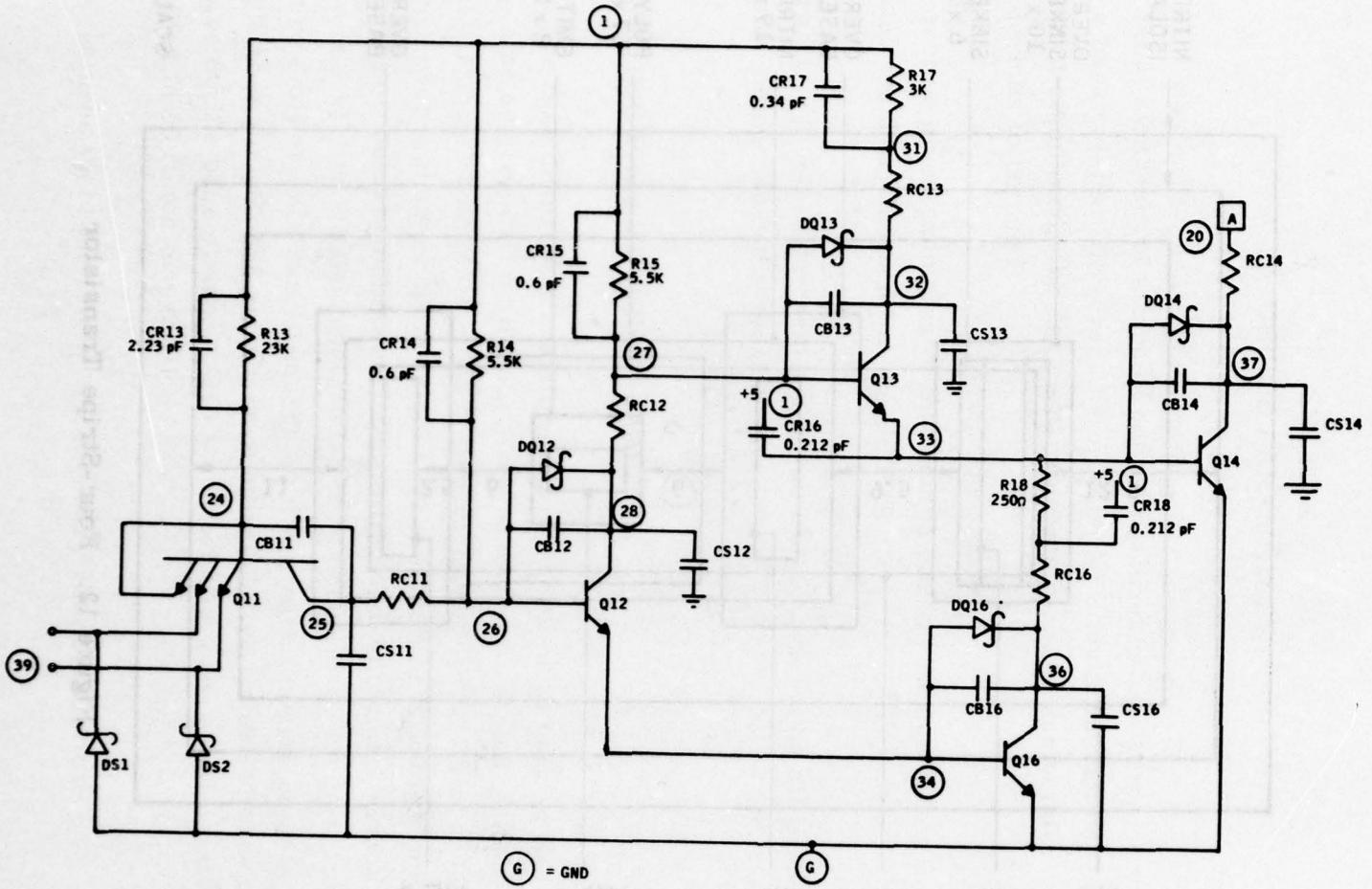


Figure 11. Circuit Diagram for Computer Simulation (Concluded)

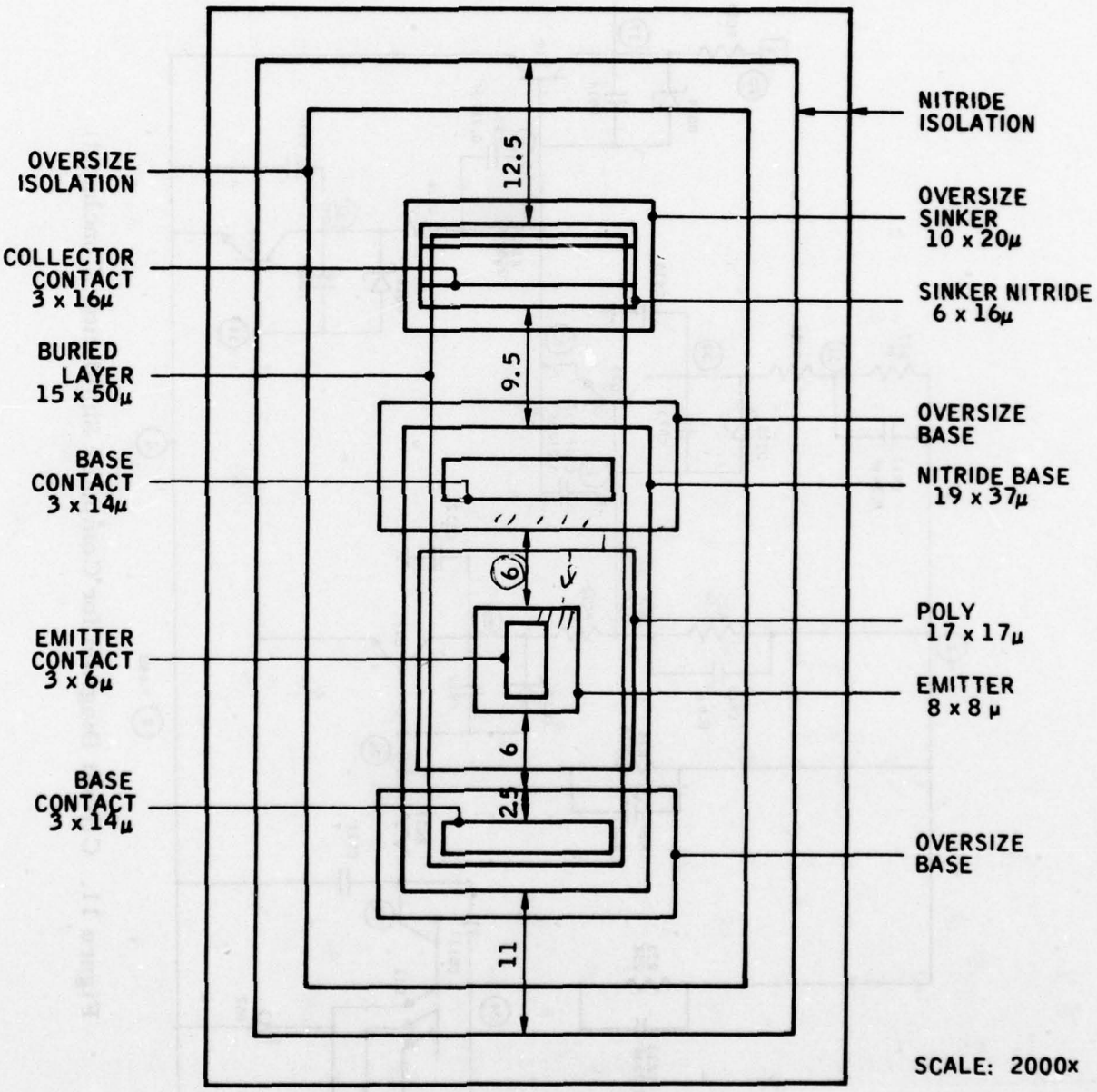


Figure 12. Four-Stripe Transistor

- Smallest ratio of emitter periphery to emitter area to ensure the best V_{BE} matching
- Wide bases relative to emitter width provides low resistance and effective use of all four emitter edges.

This structure has more base-collector capacitance than single-base structures or BEC structures with rectangular emitters, but for these linear-type operating transistors, capacitance is less important than matching or emitter efficiency.

Figure 13 shows the other style transistor used in the TTL gate portion of the FOTIC. This digital section (Q11 through Q14, Q16) requires high-speed Schottky-clamped transistors (Q15 is not used). The Schottky diodes vary in size as do the emitters, but the structure features BEC placement and rectangular emitters to minimize capacitance and provide easy Schottky diode contact.

Table 17 shows the relative transistor sizes and, in addition, includes a measure of the f_τ peak current to indicate that all transistors operate on the linear side of the peak (i.e., less than the peak shown in the Appendix, Figure A-4). The current density of the transistor used for that curve is 0.026 mA/μ^2, and when multiplied by the area of each transistor, yields a number greater than or equal to the typical current flowing through the transistor.

Figure 14 shows the model used for the transistors whose parameters were derived above.

Figure 15 shows a cross section of a transistor with various equations for calculating the parameters of a transistor. Table 18 summarizes all the data generated by using Figure 15 and Table 17.

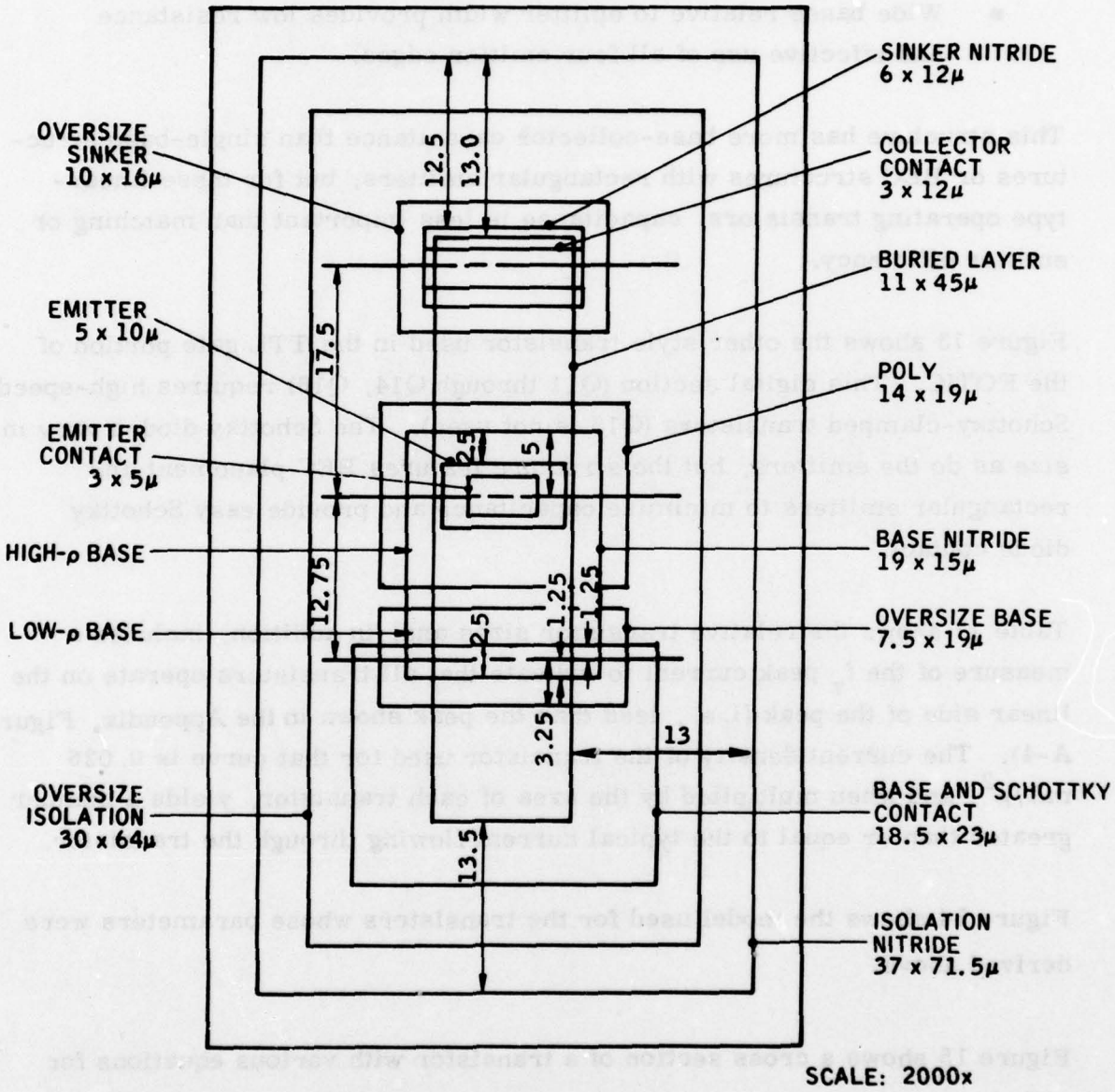


Figure 13. Layout of Schottky-Clamped Transistor Q12

TABLE 17. RELATIVE TRANSISTOR EMITTER SIZES

Emitter Size[a]	Q1 and Q3 - Q7	Q2	Q8 and Q9	Q10	Q11 and Q12 and Q16	Q13	Q14
Emitter length (μ)	10.7	10 (10.7)	75.7	535.2	12.7	25.7	75.7
Emitter width (μ)	10.7	10.7	7.7	10.7	7.7	7.7	7.7
Emitter area (μ^2)	114.5	1145.0	582.9	5695.0	97.8	197.9	582.9
Normalized area	1.0	10.0	5.0	50.0	0.85	1.7	5.0
Typical I_E (mA)	0.33	0.33	12.0	150.0	0.65	1.5	12.0
0.026 x area	3.0	30.0	15.0	150.0	2.5	5.2	15.0

[a]Dimensions are after processing.

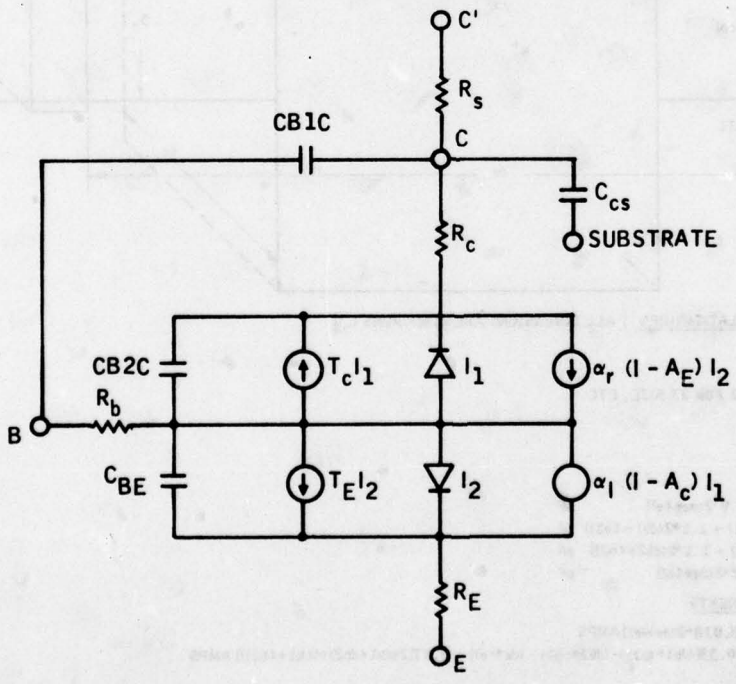
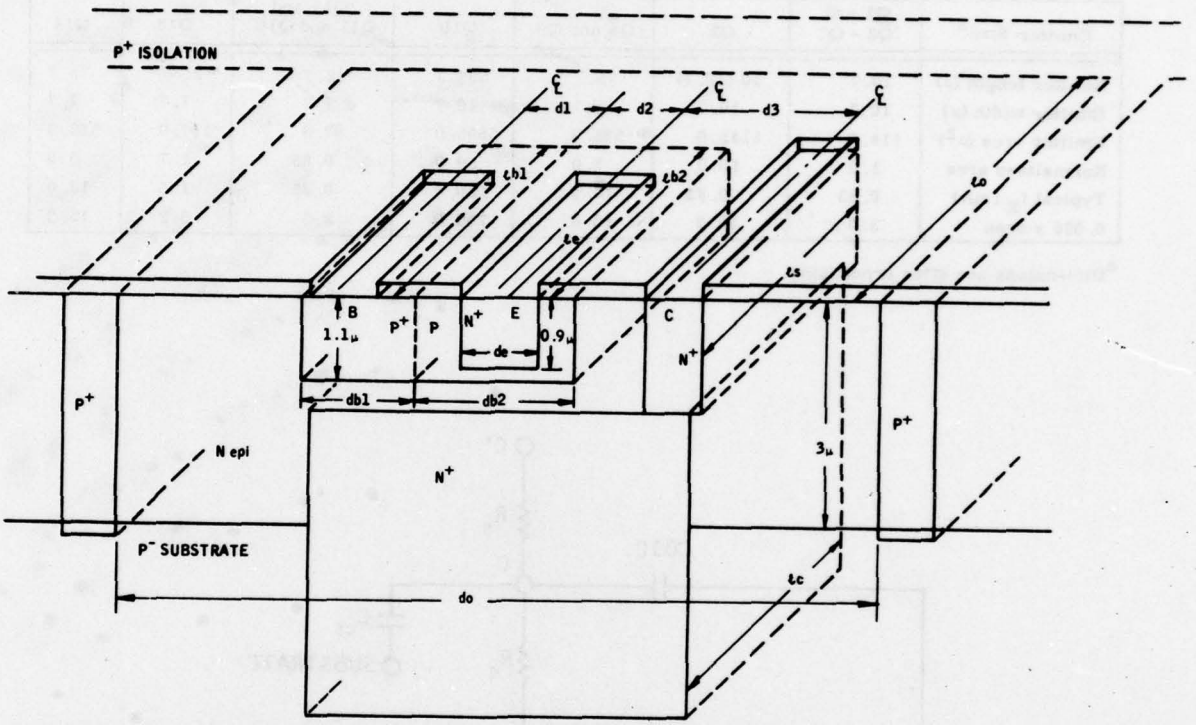


Figure 14. NPN Transistor Model



APPROXIMATE SCALING RELATIONSHIPS [ALL DIMENSIONS ARE IN MICRONS (μ)]

RESISTANCES:

RE = 0.7/N + 480/(ℓe*de)
N=1 FOR 1X SIZE, N=2 FOR 2X SIZE, ETC.
RS = 75/ℓs Ω
RC = 8.6*d3/ℓc Ω
RB1 = 266*d1/ℓb1 Ω
RB2 = 240*d2/ℓb2 Ω

CAPACITANCES:

CBE = $2.8*10^{-3}$ [de*ℓe + 0.9*2(de+ℓe)] pF
CB1C = $4.8*10^{-4}$ [(db1*ℓb1) + 1.1*2(db1+ℓb1)] pF
CB2C = $4.8*10^{-4}$ [(db2*ℓb2) + 1.1*2(db2+ℓb2)] pF
CCS = $3.1*10^{-4}$ [(do*ℓo) + 3*2(do+ℓo)] pF

REVERSE SATURATION CURRENTS:

IES = $1.2*10^{-18}$ [(de*ℓe) + 0.018*2(de+ℓe)] AMPS
ICS = $2.4*10^{-19}$ [(de*ℓe) + 0.35[(db1*ℓb1) + (db2*ℓb2) - (de*ℓe)] + 0.37[2(db1+db2)+(ℓb1+ℓb2)]] AMPS

Figure 15. Cross-Sectional View of Transistor With Equations for Calculating Transistor Parameters

TABLE 18. TRANSISTOR PARAMETERS

Parameter	Q1 and Q3 - Q7	Q2	Q8 and Q9	Q10	Q11	Q12	Q13	Q14	Q16	Units
Base resistance, R_B [a]	110.0	24.0	38.0	6.5	421.0	181.0	105.0	40.0	181.0	Ω
Collector resistance, R_C	9.3	1.7	2.6	0.48	44.5	5.3	3.5	1.1	5.3	Ω
Emitter resistance, R_E	4.9	0.49	0.96	0.098	5.6	5.6	3.1	1.5	5.6	Ω
Sinker resistance, R_s	3.0	2.0	0.9	0.14	3.6	3.6	2.3	0.9	3.6	Ω
Emitter saturation, I_{ES}	1.38	13.8	7.03	68.9	1.18	1.18	2.39	7.03	1.18	10^{-16}A
Collector saturation, I_{CS}	0.967	5.14	2.74	21.3	1.6	0.59	1.05	2.65	0.54	10^{-16}A
Base-emitter capacitance, C_{BE}	0.43	3.8	2.1	19.0	0.38	0.38	0.72	2.05	0.38	pF
Collector-base internal, C_{B1C}	0.36	1.1	0.62	4.1	0.15	0.12	0.19	0.48	0.12	pF
Collector-base external, C_{B2C}	0.16	1.0	0.5	3.8	0.87	0.12	0.19	0.57	0.12	pF
Collector-Sub capacitance, C_{CS}	0.4	1.8	0.75	6.5	0.6	0.35	0.5	0.91	0.88	pF
Normal beta	80.0	---	---	---	---	---	---	---	---	---
Reverse beta	5.0	---	---	---	---	---	---	---	---	---

[a] $R_b = R_{B1} + R_{B2}$.

SCHOTTKY DIODE PARAMETERS

The measured parameter values of a typical Schottky diode at 25°C whose area is 144 μ^2 are as follows:

$$V_{forward} = 0.670 \text{ at } 1 \text{ mA}, \; R_{SH} = 135\Omega, \; C_{SH} = 0.12 \text{ pF}$$

To determine the per unit area parameters, start with the contact potential, V_c:

$$V_c = \frac{n K T}{q}$$

where

n = 1.1
K = Boltzman's constant
T = °Kelvin
q = Electronic charge.

Thus,

V_c = 0.020657 at -55°C

V_c = 0.028237 at +25°C

V_c = 0.040082 at +150°C

The reverse saturation current, I_s, is given as:

$$I_s = I_{SH}\, e^{-\frac{V_{SH}}{V_c}}$$

where I_{SH} and V_{SH} are the current and voltage of the Schottky diode without series resistance. Thus,

$$V_{SH} = 0.670 - (135)(0.001) = 0.535V$$

The capacitance is not a function of temperature, but the resistance has a +0.25%/°C temperature coefficient. Taking into account the 144 μ^2 area, the per unit parameters as a function of temperature is listed in Table 19.

TABLE 19. PER UNIT AREA SCHOTTKY PARAMETERS

Parameter	-55°C	+25°C	+125°C	Units
I_o	1.2×10^{-19}	4×10^{-14}	1.2×10^{-9}	A/μ^2
R_o	1.52×10^{4}	1.9×10^{4}	2.5×10^{4}	$\Omega\text{-}\mu^2$
C_o	---	8.3×10^{-4}	---	pF/μ^2

Based on the area of each Schottky diode, Table 20 lists the parameters of the various transistor Schottky diodes.

TABLE 20. SCHOTTKY PARAMETERS

Parameter	Q12	Q13	Q14	Q16	Units
Reverse saturation, I_s	16.6	16.6	25.0	33.0	$10^{-12}A$
Resistance, R_{SH}	45.7	45.7	30.5	22.8	Ω
Capacitance, C_{SH}	0.34	0.34	0.52	0.68	pF

Figure 16 shows the Schottky diode model used for simulation.

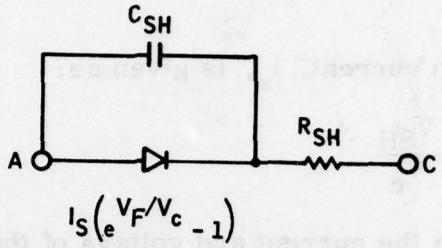


Figure 16. Schottky Diode Model

RESISTOR DESIGN

As explained in the Appendix, there are two base resistivities, high-ρ and low-ρ. In addition, there is an emitter resistivity used for output current-limiting resistors. Each type has its own characteristics which influence how actual resistor values are obtained.

High-ρ Resistors

A typical high-ρ implanted resistor is shown in Figure 17. The resistance is largely determined by the length, x, of the high-ρ implant region. To calculate the actual resistance, the final length (x - Δx) and width, W + ΔW, must be determined. The end effects cannot be ignored. A contact resistance and end resistance factor due to the low ρ diffusion must be accounted for. The number of squares of bulk high-ρ resistance is given by:

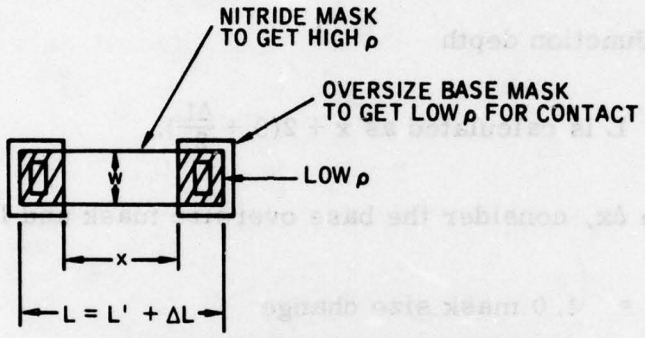
$$\square = \frac{x - \Delta x}{W + \Delta W}$$

The bulk resistance, R_b, is given by

$$R_b = 500 \times \square = 500 \frac{(x - \Delta x)}{W + \Delta W}$$

The contact resistance per end is given by $\frac{(125\ \Omega\mu)}{\ell_c}$, where ℓ_c is the length of the contact after oxide cut.

The low ρ resistance per end is given by $(\frac{\ell_1\ 50}{W_1})\ \Omega$, where ℓ_1 is the spacing from contact edge to low-ρ diffusion edge, and W_1 is the same as W + ΔW.



$\Delta x = \Delta w =$ 1.0 MASK
0.5 PHOTO PROCESS (NITRIDE)
+ 1.4 DIFFUSION
2.9 μ

$\Delta L =$ 1.0 MASK
2.1 PHOTO PROCESS (OVERLAY MASK)
+ 1.4 OUT DIFFUSION
4.5 μ

$L' = x + 2\,(3 + 3 + 2)$

Figure 17. High-ρ Resistor Layout

Therefore:

$$R_T = 500\,\frac{(x - \Delta x)}{(W + \Delta W)} + 2\left[\frac{125}{\ell_c} + 50\,\frac{\ell_1}{W_1}\right]$$

The equation for capacitance of a resistor is given by:

$$C = 4.8 \times 10^{-4} \cdot A\ pF$$

where A is the total junction area in μ^2 and is given by:

$$A = LW + 2(1.1)\,[L + W]$$

where

L = Total diffusion length = Layout dimensions + ΔL

W = Total diffusion width = W + ΔW

1.1 = Junction depth

Alternately, L is calculated as $x + 2(8 + \frac{\Delta L}{2})$.

To calculate Δx, consider the base oversize mask and low ρ:

Δx = 1.0 mask size change
+ 0.5 photo process size change
+ 1.4 out diffusion both sides

Therefore, $\Delta x = 2.9$.

To calculate ΔW, consider the nitride mask, and high ρ:

ΔW = 1.0 mask size change
+ 0.5 photo process size change
+ 1.4 out diffusion both sides

Therefore, $\Delta W = 2.9$.

To calculate ℓ_c, the final contact width, sum up these dimensions:

6.0 layout
+ 1.0 nominal mask change
+ 2.0 photo process change

Therefore, $\ell_c = 9.0\ \mu$.

To calculate ΔL, take the sum of the size changes for L, determined by both the nitride and oversize masks:

$$\begin{aligned} &1.0 \text{ mask size change} \\ &+ 2.1 \text{ photo process change on nitride} \\ &\underline{+ 1.4} \text{ out diffusion for both ends} \end{aligned}$$

Therefore, $\Delta L = 4.5\ \mu$.

To calculate ℓ_1, the spacing between the contact and the low-ρ diffusion edge, we must calculate the relative feature edge shifts.

$$\begin{aligned} &3.0 \text{ = layout spacing} \\ &- 1.5 \text{ = contact edge change, one side} \\ &\underline{+ 1.45} \text{ = low-}\rho\text{ edge change, one side} \end{aligned}$$

Therefore, $\ell_1 = 2.95\ \mu$.

We can now calculate the resistance and capacitance for a given layout. For the FOTIC design, a layout width of 10 μ was used. Thus, the total resistance is:

$$R_T = 500 \frac{(x - 2.9)}{12.9} + 2\left[\frac{125}{9} + \frac{2.95}{12.9} \cdot 50\right]$$

$$R_T = 38.76\,(x - 2.9) + 50.64$$

Therefore, starting with the resistor value, the layout dimension x can be determined by:

$$x = \frac{R_T - 50.64}{38.76} + 2.9$$

The spacing ℓ_1 was incorrectly estimated to be 2.0 μ, so the resistance listed in Table 21 was calculated from this equation:

$$x = \frac{R_T - 43.2}{38.76} + 2.9$$

The capacitance is now determined from the layout dimensions:

$$C = 4.8 \times 10^{-4} [(x + 2(8) + 4.5)(12.9) + 2.2(x + 20.5 + 12.9)]$$

$$= 4.8 \times 10^{-4} [15.1 (x + 20.5) + 28.38]$$

$$= 0.00725 (x + 20.5) + 0.0136 \text{ pF}$$

The length ΔL was incorrectly estimated to be 2.9, so the capacitance listed in Table 21 was calculated from this equation:

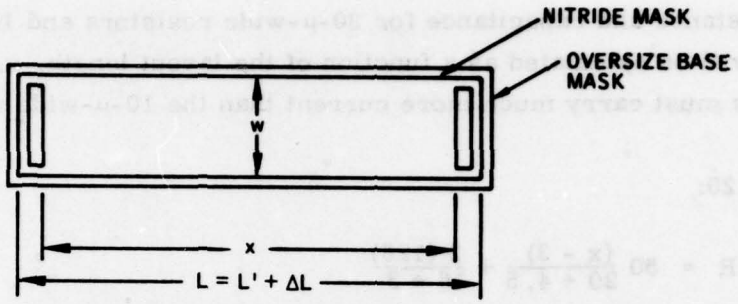
$$C = 0.00725 (x + 18.9) + 0.0136 \text{ pF}$$

Low-ρ Resistors

A typical low-ρ resistor is shown in Figure 18. The resistance is determined by the number of squares of resistance plus contact resistance. The final length, x - Δx, and width, W + ΔW, will be calculated from the Δx and ΔW shown in Figure 18.

- The number of squares is $\frac{x - \Delta x}{W + \Delta W}$.
- The bulk resistance is $50 \frac{(x - \Delta x)}{(w + \Delta w)}$.
- The contact resistance is $2 \times \frac{125\ \Omega/\mu}{W_c + \Delta W_c}$.

where W_c is the layout width of the contact and $\Delta W_c = 3\ \mu$ is the total size change of the contact.



Δx = 1.0 MASK
+2.0 PHOTO PROCESS (CONTACT)
3.0μ

Δw = 1.0 MASK
2.1 PHOTO PROCESS (NITRIDE AND OVERLAY)
1.4 OUT DIFFUSION
4.5μ

$\Delta L = \Delta w$

$W = w + \Delta w$

$L' = x + 2(3 + 2) = x + 10$

Figure 18. Low-ρ Resistor Layout

The capacitance is calculated for low-ρ resistors from

$$C = C_o \cdot A$$

where

$$C_o = 4.8 \times 10^{-4}\ pF/\mu^2$$

$$A = (L + W) + 2(1.1)(L + W)$$

where

$$L = x + 10 + \Delta L$$

and

$$W = w + \Delta W = w + 4.5$$

The resistance and capacitance for 20-μ-wide resistors and 10-μ-wide resistors will be calculated as a function of the layout length, x. The 20-μ resistors must carry much more current than the 10-μ-wide resistors.

For w = 20:

$$R = 50\,\frac{(x - 3)}{20 + 4.5} + \frac{2\,(125)}{16 + 3}$$

$$R = 2.0408(x - 3) + 13.16$$

Starting with the resistor value, the layout dimension is calculated:

$$x = R - \frac{13.16}{2.0408} + 3.0$$

The capacitance for 20-μ resistors is C_{20}:

$$C_{20} = 4.8 \times 10^{-4}\,[(x + 10 + 4.5)(24.5) + 2(1.1)(x + 14.5 + 24.5)]$$

$$C_{20} = 0.012816(x + 14.5) + 0.02587$$

For w = 10 μ:

$$R = \frac{50(x - 3)}{14.5} + \frac{2(125)}{6 + 3}$$

$$R = 3.448(x - 3) + 27.78$$

Therefore,

$$x = \frac{R - 27.78}{3.448} + 3$$

The capacitance for 10-μ-wide resistors is

$$C = 4.8 \times 10^{-4} [(x + 10 + 4.5)(14.5) + 2(1.1)(x + 14.5 + 14.5)]$$

$$C = 4.8 \times 10^{-4} [x + 14.5) + 16.7 + 31.9]$$

$$C = 0.00802(x + 14.5) + 0.0153$$

A typical emitter (n^+) resistor is shown in Figure 19. The resistance is determined by the number of squares of n^+ between the contacts and the contact resistance.

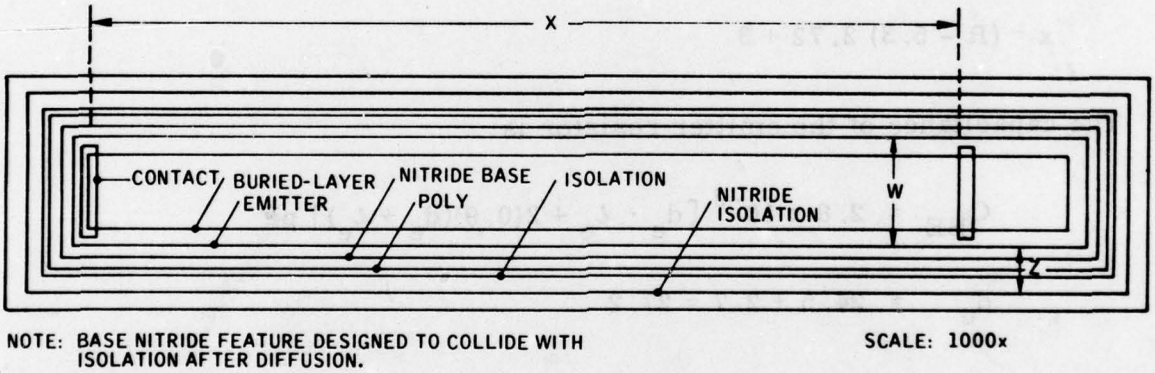


Figure 19. n^+ Resistor Layout

The number of squares is given by:

$$\square = \frac{x - \Delta x}{W + \Delta W}$$

Therefore, the bulk resistance is:

$$R_b = 10 \frac{(x - \Delta x)}{W + \Delta W}$$

The contact resistance is given by

$$R_{end} = \frac{125\ \Omega\ \mu}{W_c + 3} = \frac{125}{23.5} = 5.3\ \Omega$$

$$R = \frac{(x - 3)}{27.2} + 5.3$$

where

$$x = (R - 5.3)\ 2.72 + 3$$

The capacitance of the emitter resistor is:

$$C_{BE} = 2.8 \times 10^{-3} [d_e \cdot \ell_e + 2(0.9)(d_e + \ell_e)]\ pF$$

$$d_e = 24.5 + 2.7 = 27.2$$

$$\ell_e = 221 + 2.7 = 224.7$$

Therefore, $C_{BE} = 18.3$ pF.

Table 21 is a summary of the values and sizes calculated using the preceding design information.

TABLE 21. RESISTOR SIZE AND CAPACITANCE

Resistor Number	Value (Ω)	Type	Number in Series or Parallel	x	Capacitance of Each	Total Capacitance
R1	176.5	High-ρ	4p	20.0	0.30	1.20
R2	3,433.0	High-ρ	5s	19.5	0.20	1.46
R3	3,433.0	High-ρ	5s	19.5	0.29	1.46
R4	6,585.0	High-ρ	1	171.5	1.39	---
R5	191.0	High-ρ	4p	21.5	0.31	1.23
R6	1,560.0	High-ρ	1	42.0	0.46	---
R7	100,000.0	High-ρ	3s	218.5	1.73	5.20
R8	87.2	Low-ρ (20 μ)	2p	82.0	1.26	2.52
R9	390.0	Low-ρ (20 μ)	1	187.5	2.61	---
R10	72.4	n+	1	185.5	1.5	18.3
R11	36.75	n+	2p	188.5	1.5	36.6
R12	24.5	n+	3p	188.5	1.5	54.9
R13	23,000.0	High-ρ	3s	199.5	1.60	4.79
R14	5,500.0	High-ρ	1	143.5	1.19	---
R15	5,500.0	High-ρ	1	143 5	1.19	---
R17	3,000.0	High-ρ	1	79.0	0.72	---
R18	250.0	Low-ρ (10 μ)	1	63.5	0.64	---
R19	53.0	Low-ρ (20 μ)	1	22.5	0.31	---

RESISTOR MODELS

Model for Resistors in Common Epi

The model for a resistor in a common epi boat is shown in Figure 20. The cross section shows the resistor boat tied to the most positive point in the circuit. The distributed capacitance of the pn junction is lumped with half at each end.

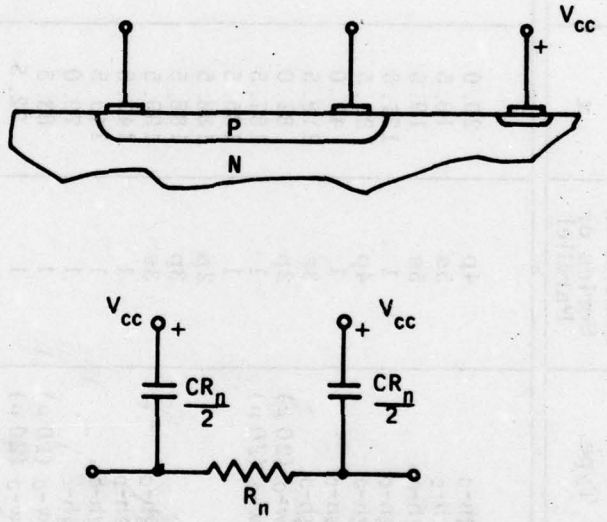


Figure 20. Model for Resistor in Common Epi

Model for Resistors Individually Isolated

The model for a resistor in its own epi boat is shown in Figure 21. The cross section shows the boat tied to the positive end of the resistor. The distributed capacitance is placed in parallel with the resistor.

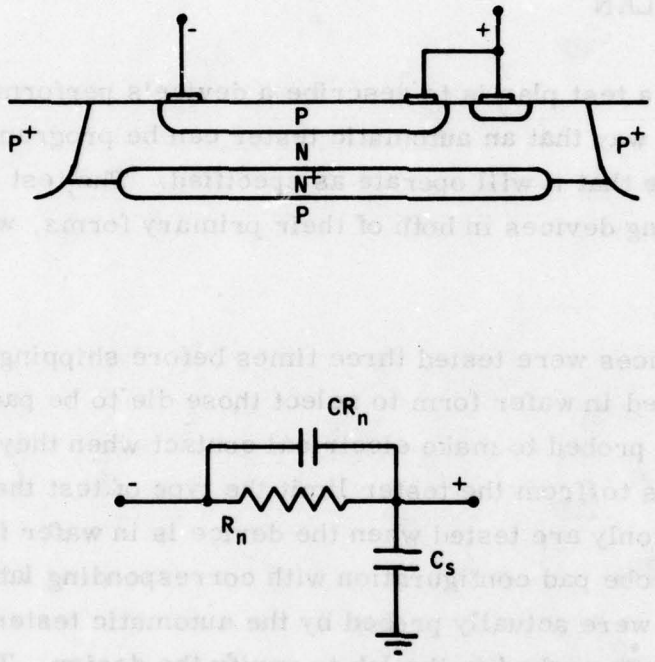


Figure 21. Model for Resistor in Separate Isolation

SECTION VI
TESTING AND PACKAGING

FOTIC TEST PLAN

The purpose of a test plan is to describe a device's performance characteristics in such a way that an automatic tester can be programmed to test the device to ensure that it will operate as specified. The test plan must be usable for testing devices in both of their primary forms, which are wafers and packages.

The FOTIC devices were tested three times before shipping. First, the devices were tested in wafer form to select those die to be packaged. Because the die must be probed to make electrical contact when they are in wafer form, long lines to/from the tester limit the type of test that can be made. D-C conditions only are tested when the device is in wafer form. Figure 22 shows the probe pad configuration with corresponding labeling. Only the numbered pads were actually probed by the automatic tester. The other smaller pads were probed in the lab to verify the design. The a-c type tests are made on packaged die only, because the input and output impedances can be controlled relatively easily.

The second time the FOTIC devices were tested was after they were packaged and the environmental screens, except burn-in, had been performed. (See Table 22.) At that time, all d-c and a-c tests were performed to select the devices to be burned in. After burn-in, the devices were tested a third and final time just prior to shipping.

The following test plan is implemented on an automatic tester that was used as described above. It contains d-c tests (1 through 119) and a-c tests

(120 through 143). In addition, two sets of d-c tests are intermingled, one for the 8-pin TO-99 package that must use external discrete load resistors and one for the 14-pin DIP that uses on-chip resistors. A description of the tabulated test information (Table 22) is provided to explain the purpose of each test and to make it easier to correlate the test plan to the device specification and the analysis.

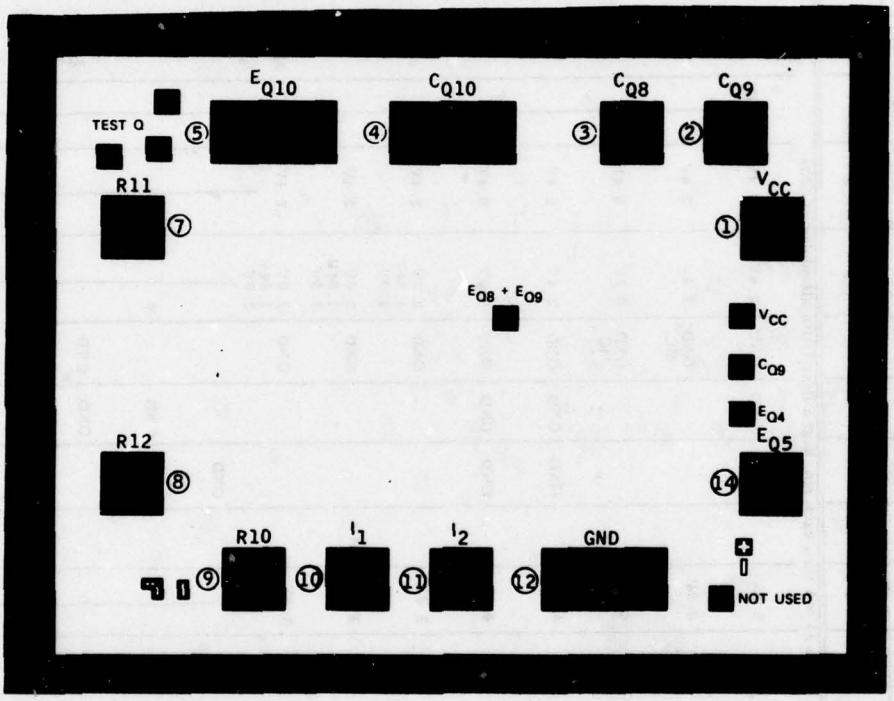


Figure 22. FOTIC Probe Pad Locations

Notes for Table 1 (Test Plan Listing)

Note 1--For "150-mA load," connect all three on-chip resistors (R_{10}, R_{11}, and R_{12}) to ground for wafers and DIPs. For TO-99s, use $R_{External}$ = 12.06 Ω.

TABLE 22. TEST PLAN LISTING FOR DEVICE NO. 2144, FIBER OPTIC TRANSMITTER INTEGRATED CIRCUIT (FOTIC)

Test No.	Pin / Pad / Test	1	2	3	4	5	7	8	9	10	11	12	14	Note 8	Limits		
		V_{cc}	C_{Q9} C_{Q14} B_{Q10}	C_{QB}	C_{Q10}	E_{Q10}	R11	R12	R10	I_1	I_2	GND	E_{Q5}	Notes	Min.	Max.	Units
1-12	Probe contact	Force ±1 mA thru each pin, 1 at a time, with all others at GND.												1, 2	---	1.0	V
13	Worst-case supply current	5.5V MC			5.5V		GND	GND	GND	2.4V	2.4V	GND		9	100	200 190 200	mA
14	Max. over-voltage inputs high	7.0V			6.0V				GND MC	2.4V	2.4V				10	70 55 70	mA
15	Max. over-voltage inputs low	7.0V			6.0V				GND MC	0.4V	0.4V				10	50 50 50	mA
16	I_{cc} inputs high	5.5V MC			4.3V		GND	GND	GND	2.4V	2.4V				10	21.71 21.44 22.94	mA
17	I_{cc} inputs low	5.5V MC			4.3V		GND	GND	GND	0.4V	0.4V				10	37.95 36.46 36.46	mA
18	Output current 25-mA step	5.5V			3.8V				GND	2.0V 1.84V 2.0V	2.4V			3, 4, 5	See Table 23 or 24		
19	V_{Q10E} 25-mA step	5.5V			3.8V	MV			GND	2.0V 1.84V 2.0V	2.4V				See Table 25		
20	V_{Q5E} 25-mA step	5.5V			3.8V				GND	2.0V 1.84V 2.0V	2.4V		MV		See Table 25		
21 22 23	Repeat tests 18-20, 50-mA step						GND								See Tables 23, 24, or 25		
24 25 26	Repeat tests 18-20, 75-mA step							GND							See Tables 23, 24, or 25		
27 28 29	Repeat tests 18-20, 100-mA step							GND	GND						See Tables 23, 24, or 25		
30 31 32	Repeat tests 18-20, 125-mA step						GND	GND							See Tables 23, 24, or 25		
33 34 35	Repeat tests 18-20, 150-mA step						GND	GND	GND						See Tables 23, 24, or 25		

TABLE 22. TEST PLAN LISTING FOR DEVICE NO. 2144, FIBER OPTIC TRANSMITTER INTEGRATED CIRCUIT (FOTIC) -- CONTINUED

Test No.	Pin / Pad / Test	1	2	3	4	5	7	8	9	10	11	12	14	Note 8	Limits		
		V_{CC}	C_{Q9} C_{Q14} B_{Q10}	C_{Q8}	C_{Q10}	E_{Q10}	R11	R12	R10	I_1	I_2	GND	E_{Q5}	Notes	Min.	Max.	Units
36 ↓ 52	Repeat tests 18-35; interchange inputs	5.5V			3.8V					2.4V	2.0V 1.84V 2.0V	GND			See Tables 23, 24, or 25		
53 ↓ 89	Repeat tests 18-52 (V_{CC} = 4.5V)	4.5V			3.8V										See Tables 23, 24, or 25		
90	Output "OFF" current	5.5V			4.3V MC				GND	0.4V	0.4V			6	1.0	40 40 50	µA
91	Pipes	5.5V	GND		4.3V MC				GND	0.4V	0.4V				0	30 30 40	µA
92	Input clamp voltage	4.5V								-12 mA MV	GND				-1.2	-0.5	V
93	Schottky data	4.5V								-10 mA MV	GND				Data collection		
94	Schottky data	4.5V								-1 mA MV	GND				Data collection		
95	Schottky data	4.5V								-0.1 mA MV	GND				Data collection		
96	Schottky data	4.5V								-0.01 mA MV	GND				Data collection		
97 ↓ 101	Repeat tests 92-96; interchange inputs	4.5V								GND	MV				Same as for tests 92-96		
102	Maximum input current	5.5V								5.5V MC	GND				0	1.0	mA
103	Maximum input current									GND	5.5V MC				0	1.0	mA
104	Input leakage current									5.5V MC	5.5V MC				0	1.0	µA
105	High state input current									2.4V MC	GND				0	40 35 40	µA
106	High state input current									GND	2.4V MC				0	40 35 40	µA

TABLE 22. TEST PLAN LISTING FOR DEVICE NO. 2144, FIBER OPTIC TRANSMITTER INTEGRATED CIRCUIT (FOTIC) -- CONTINUED

Test No.	Pin / Pad / Test	1	2	3	4	5	7	8	9	10	11	12	14	Note 8	Limits		
		V_{cc}	C_{Q9} C_{Q14} B_{Q10}	C_{Q8}	C_{Q10}	E_{Q10}	R11	R12	R10	I_1	I_2	GND	E_{Q5}	Notes	Min.	Max.	Units
107	Low state input current	5.5V								0.4V MC	2.4V	GND			-1.60 -1.36 -1.60	-0.5	mA
108	Low state input current									2.4V	0.4V MC				-1.60 -1.36 -1.60	-0.5	mA
109	Input breakdown									1 mA MV	GND				5.5	---	V
110	Input breakdown									GND	1 mA MV				5.5	---	V
111	Input threshold								1 mA	2.4V	Ramp MV				0.8 1.05 0.8	2.0 1.84 2.0	V
112	Input threshold								1 mA	Ramp MV	2.4V				0.8 1.05 0.8	2.0 1.84 2.0	V
113	Collector of Q9	5.0V	MV							2.4V	2.4V				2.45	2.93	V
114	Collector of Q9	5.0V	MV							GND	GND				0.2	0.43	V
115	Collector of Q8	5.0V		MV						GND	GND				2.90	4.35	V
116	Collector of Q8	5.0V		MV						2.4V	2.4V				3.48	4.55	V
117	Value of R10					2.0V MC			GND						65.2	79.6	Ω
118	Value of R11					2.0V MC	GND								33.1	40.4	Ω
119	Value of R12					2.0V MC		GND							22.1	27.0	Ω

TABLE 22. TEST PLAN LISTING FOR DEVICE NO. 2144, FIBER OPTIC TRANSMITTER INTEGRATED CIRCUIT (FOTIC) -- CONCLUDED

Test No.	Pin / Pad / Test	1	2	3	4	5	7	8	9	10	11	12	14	Note 8	Limits		
		V_{cc}	C_{Q9} C_{Q14} B_{Q10}	C_{Q8}	C_{Q10}	E_{Q10}	R11	R12	R10	I_1	I_2	GND	E_{Q5}	Notes	Min.	Max.	Units
120	Normalize voltage swing	5.5V								2.4V		GND		7	---	---	---
121	Rise time														0	7 6 7	ns
122	Fall time														0	10 8 10	ns
123	Delay rise														0	15 10 15	ns
124	Delay fall														0	15 10 15	ns
125	Delay differential														0	5 3.5 5	ns
126 ↓ 131	Repeat tests 120-125; interchange inputs	5.5V													Same as tests 120-125		
132 ↓ 143	Repeat tests 120-131 (V_{cc} = 4.5V)	4.5V													Same as tests 120-131		

Calculate (Test 123 - Test 124) = Differential |Absolute Value|

change of the contact.

Note 2--When three limit values are given, the top one is for -55°C, the next for 25°C, and the bottom for 150°C junction temperature (T_j).

Note 3--For tests 18 through 89, the current in C_{Q10} is measured for all combinations of two inputs and two supply voltages. Test 18 through 35 must be repeated four times. Limits are shown in Table 23 for wafers and 14-pin DIPs.

TABLE 23. OUTPUT CURRENT LIMITS FOR ON-CHIP RESISTORS

Nominal Current Step, mA	Resistor Tied to Ground	Limits				Units
		25°C		-55°C or 125°C		
		Minimum (±16%)	Maximum (±16%)	Minimum (±20%)	Maximum (±20%)	
25	R10	21	29	20	30	mA
50	R11	42	58	40	60	mA
75	R12	63	87	60	90	mA
100	R10 and R12	84	116	80	120	mA
125	R11 and R12	105	145	100	150	mA
150	R10, R11, and R12	126	174	120	180	mA

Note 4--Tests 18 through 89 should be replaced with new limits from Table 24 for external current-setting resistors used for TO-99 packages. Table 24 also specifies the resistor values to be used.

Note 5--The voltages on the emitters of Q10 and Q5 should be measured and logged for parameter distributions, at each supply voltage and temperature. The limits are given in Table 25.

TABLE 24. OUTPUT CURRENT LIMITS FOR EXTERNAL RESISTORS

External Resistor, Ω	Limits			Units
	25°C (±8%)	-55°C (±10%)	+150°C (±10%)	
73.12	25	22.6	28.75	mA
36.45	50	45.2	57.50	mA
24.25	75	67.8	86.25	mA
18.15	100	90.4	115.00	mA
14.50	125	113.0	143.75	mA
12.06	150	135.6	172.50	mA

TABLE 25. VOLTAGE AT EQ_{10} AND EQ_5 FOR DATA COLLECTION

Temperature (°C)	Limits					
	EQ_{10} (Volts) (±15%)			EQ_5 (Volts) (±15%)		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
- 55	1.429	1.681	1.933	1.433	1.686	1.939
+ 25	1.580	1.859	2.139	1.593	1.875	2.156
+125	1.764	2.075	2.386	1.796	2.113	2.430

Note 6--The R_{Ext} = 18.15 Ω for TO-99s from E_{Q10} to GND.

Note 7--Test at 4.5V and 5.5V at -55°, +25°, and +125°C. The first test is used to normalize the voltage swing.

Note 8--The pin numbers shown at the top of each column are for 14-pin DIPs. The TO-99 packages and wafers have different pin configurations.

Note 9--

MC = Measure Current

MV = Measure Voltage

Tests 1 Through 12, Probe Contact/Pin Continuity

There are 12 probe pads. The test consists of tying all pads to ground, except one, and forcing ±1 mA through that one. A test limit of |1.0| volt will exceed one diode drop to ground over the temperature range.

Note: Force 1 mA into each pin, to ground, one at a time. Limit the supply to 5V. Measure < 1V.

Test 13, Worst-Case Supply Current

This tests for the maximum supply current with a 150-mA nominal load, and includes both IC biasing current and the LED driver current in the collector of Q10. To set the current for wafers and 14-pin DIPs, use the three on-chip resistors. Use an external resistor = 12.06 Ω for TO-99 packages.

Note: V_{cc} = +5.5V. $V_1 = V_2$ = 2.40V.
R10, R11, R12 to ground. C_{Q10} to V_{cc} directly.
Limit < 200 mA at -55°C and +125°C, 190 mA at 25°C.

Tests 14 and 15, Maximum Supply Overvoltage, Inputs High/Low

The chip is required to withstand 7V, but not necessarily operate there. To minimize total chip power, the output stage will be biased using the highest value load resistor, R10. Apply 7V to V_{cc} and 6V to C_{Q10}. Failure of the part would cause the supply current to increase considerably. Measure the current in ground. See Table 26.

TABLE 26. MAXIMUM SUPPLY OVERVOLTAGE

Temperature (°C)	On-Chip Resistor to Ground	TO-99 Package External Resistor Value	Limit with Inputs = 2.4V (Test 14)	Limit with Inputs = GND (Test 15)
- 55	R10	73.12Ω	70 mA	50 mA
+ 25	R10	73.12Ω	55 mA	50 mA
+125	R10	73.12Ω	70 mA	50 mA

Tests 16 and 17, Maximum Chip Current (I_{cc}), Inputs High/Low

These tests are for the maximum current from the power supply, excluding the LED (collector of Q10) current. Bias C_{Q10} to 4.3V. Test for both input states using 0.4 and 2.4V. Set V_{cc} = 5.5V. Connect all internal resistors (R10, R11, and R12) to ground or use a 12.06-Ω external resistor for TO-99s. See Table 27.

TABLE 27. MAXIMUM CHIP CURRENT

Temperature (°C)	Limit with Inputs = 2.4V (Test 16)	Limit with Inputs = GND (Test 17)	Units
- 55	21.71	37.95	mA
+ 25	21.44	36.46	mA
-125	22.94	36.46	mA

Tests 18 Through 89, Output High State Current and Voltage Levels

The output high state current is tested for each of the programmable current steps from 25 mA to 150 mA using the on-chip resistors or external resistors for TO-99s. A guard band (±2 percent) is placed on the room temperature test value to ensure good yield over the temperature range. The test described using an external resistor is for the TO-99, since the output can be tested using an external resistor only. The worst-case logic "1" input voltage is used to assure worst-case output current. See Table 28.

Table 23 shows the output limits for various resistor connections. Since there are two inputs and the limits must be checked at two supply voltages, tests 18 through 35 must be repeated four times.

Table 24 shows the limits which apply when an external resistor is used. Since the resistor is constant over the temperature range, the limits have been adjusted and the nominal value is given.

TABLE 28. OUTPUT HIGH STATE VOLTAGE LEVELS

Temperature (°C)	ON Input Level (V)
+25	1.84
-55 or +125	2.0

Note: Set the other input at 2.4V for all cases. The collector of Q10 is biased at 3.8V.

Table 25 gives the voltages at the emitters of Q10 (E_{Q10}) and Q5 (E_{Q5}) to be tested for data collection.

Test 90, Low-Level Output "Off" Current

This test is to be made with both inputs low at 0.4V. The output current is measured with C_{Q10} biased at 4.3V, V_{cc} to 5.5V. Use external resistor = 73.12 Ω or connect on-chip resistor, R10, to ground. See Table 29.

TABLE 29. LOW-LEVEL OUTPUT OFF CURRENT

Temperature (°C)	Minimum	Maximum	Units
+25 and -55	1	40	μA
+125	1	50	μA

Test 91, Pipes

Turn Q10 off by applying 0V to the base. This test looks for pipes from emitter to collector. See Table 30.

TABLE 30. TEST FOR PIPES

Temperature (°C)	Limits		Units
	Minimum	Maximum	
+25 and -55	0	40	μA
+125	0	50	μA

Tests 92 and 97, Input Clamp Voltage

The inputs are tested for clamping of negative signals. With the supply voltage, V_{cc}, at 4.5V, and one input at ground, force -12 mA into the other input. Do this for both inputs.

Limits: -1.2V at +25°, -55°, and +125°C.

Tests 93 Through 96 and 98 Through 101, Data Collection

These tests are for data collection. Test at 10 mA, 1 mA, 100 μA, and 10 μA and measure the Schottky voltage on each input.

Tests 102 and 103, Maximum Voltage Input Current

Each input is set to 5.5V while the other is at ground. The V_{cc} supply should be set at 5.5V. Measure the input current. Do this for both inputs.

Note: $I_I < 1.0$ mA at all temperatures.

Test 104, Leakage Current of Input Transistor

Tie both inputs to +5.5V and measure the input current.

Note: $I_I < 1.0$ mA at all temperatures.

Tests 105 and 106, High State Input Current

One input is set at 2.4V and tested for input current with the other input grounded. Both inputs are to be tested. See Table 31.

TABLE 31. HIGH STATE INPUT CURRENT

Temperature (°C)	Maximum Limit	Units
+25	35	μA
-55 and +125	40	μA

Tests 107 and 108, Low State Input Current

Each input is set at 0.4V, one at a time, with the other input at 2.4V. The current that the 0.4V supply must sink is measured. V_{cc} = 5.5V. See Table 32.

TABLE 32. LOW STATE INPUT CURRENT

Temperature (°C)	Maximum Limit	Units
+25	-1.36	mA
-55 and +125	-1.60	ma

Tests 109 and 110, Input Breakdown at 1 mA

Each input is tested one at a time with the other grounded. +1 mA is applied and the breakdown voltage measured. The limit is ≥ 5.5V over the temperature range.

Tests 111 and 112, Input Threshold

Each input is tested by applying a voltage ramp to the input under test. The other input is at 2.4V. Record the voltage at which the gate switches. The gate switches when the current in R10 tied to ground or a 73.12 Ω external resistor reaches 1 mA. See Table 33.

External
12.06 Ω.

TABLE 33. INPUT THRESHOLD

Temperature (°C)	Limits		Units
	Minimum	Maximum	
+25	1.0	1.8	V
-55 to +150	0.8	2.0	V

Tests 113 Through 116, Collectors of Differential Amplifier

The output terminals of the differential amplifier are tested for both states of the input gate. See Table 34.

TABLE 34. DIFFERENTIAL AMPLIFIER OUTPUT TERMINALS

Parameter	V_{CQ8} [a]		V_{CQ9} [a]		Units
	Minimum	Maximum	Minimum	Maximum	
Both Inputs 2.4V	3.48	4.55	2.45	2.93	V
Both Inputs 0V	2.90	4.35	0.20	0.43	V

[a] All temperatures.

Tests 117, 118, and 119, Values of R10, R11, R12

The internal load resistors are tested by applying 2V to E_{Q10} and measuring the current through each resistor to ground. The resistance is calculated. See Table 35.

TABLE 35. VALUES OF R10, R11, R12

Resistor	Minimum[a]	Maximum[a]	Units
R10	65.2	79.6	Ω
R11	33.1	40.4	Ω
R12	22.1	27.0	Ω

[a]At +25 °C.

Dynamic Tests (Tests 120 Through 143)

These tests are to be measured on packaged parts only. An external 50-Ω load is to be used to match the equipment impedance (for both 14-pin DIPs and TO-99s).

Delays are measured between 50 percent points; rise and fall times between 10 percent and 90 percent points. Thus, the data should be normalized to calculate these points, rather than testing to absolute levels. Input pulse has a rise time of 5 ns and a minimum width of 40 ns. See Table 36.

TABLE 36. DYNAMIC TESTS

Test No.	Parameter	+25 °C at 5V	-55 °C and +125 °C at 4.5V	Units
120	Normalized test	---	---	---
121	T_R, rise time	6.0	7	ns
122	T_F, fall time	8.0	10	ns
123	$T_{D_{LH}}$, delay low to high	10.0	15	ns
124	$T_{D_{HL}}$, delay high to low	10.0	15	ns
125	$T = (T_{D_{LH}} - T_{D_{HL}})$	3.5	5	ns

Note: Test 125 is a calculation to be sure the two delays meet the specification for matching. The sequence is tested at 5.5V for each input and at 4.5V for each input. Switch the inputs between 0.4 and 2.4V.

FOTIC BURN-IN PLAN

The burn-in specification is Mil-Std-883, Method 1015, Condition B. This standard states that the parts shall undergo at least 168 hours (7 days) of 125°C ambient temperature under active conditions. The object of the burn-in is to temperature-stress the parts to "weed" out the early failures due to marginal junctions, wire bonds, etc.

The overall block diagram of the burn-in setup is shown in Figure 23. The logic board designed to operate the parts during burn-in is shown in Figure 24 and the device board wiring diagrams for the 14-pin DIP and TO-99 are shown in Figures 25 and 26.

On each device burn-in board there are 120 devices, 20 columns by 6 rows. Since the inputs to the FOTIC are TTL, only 10 FOTICs can be driven from a standard TTL gate.[9] This requres that there be 24 driver gates (see Figure 23). An open collector-type driver was used so that the inputs to the FOTIC would see the maximum voltage transition (V_{cc} to gnd) that they would be subjected to under worst-case operating conditions.

The SN5473 JK flip-flops were used for two reasons. First, the driver gate inputs had to be necked down so that the TTL load presented to the square-wave generator was minimum. Each side of the flip-flop drives six gates, and necks down the 1-kHz generator load to 2. Second, the inputs to the FOTIC needed to be interchanged for the worst-case active condition. One of the FOTIC inputs is normally enabled at a constant high input while the other input receives the changing signal. The inputs I_1 and I_2 are completely equivalent to each other, so either can act as the signal input under normal operating conditions. The inverter driving one of the flip-flops (while not really necessary) was used to keep half of the FOTIC's enable inputs opposite of the other half (i.e., one half uses I_1 as enable while the other half

[9] Both FOTIC inputs could have been tied together and driven as one TTL load, but for worst-case operation, each input is driven individually.

AD-A071 437 HONEYWELL INC MINNEAPOLIS MN SYSTEMS AND RESEARCH CENTER F/G 20/6
FIBER OPTICS TRANSMITTER INTEGRATED CIRCUIT DEVELOPMENT.(U)
JUL 78 B R ELMER F33615-76-C-1280
UNCLASSIFIED F0470-FR AFAL-TR-78-107 NL

2 OF 2
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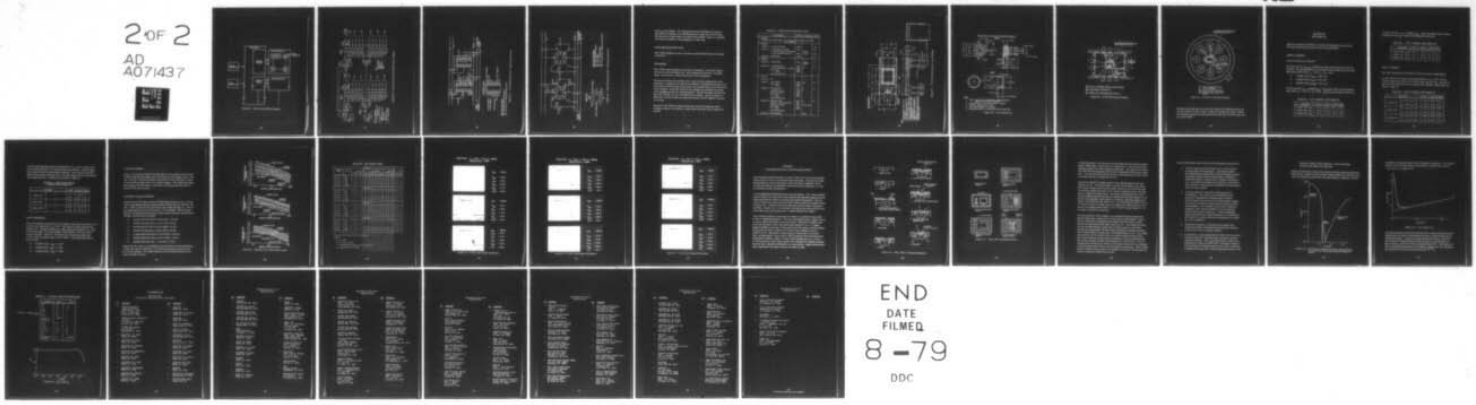

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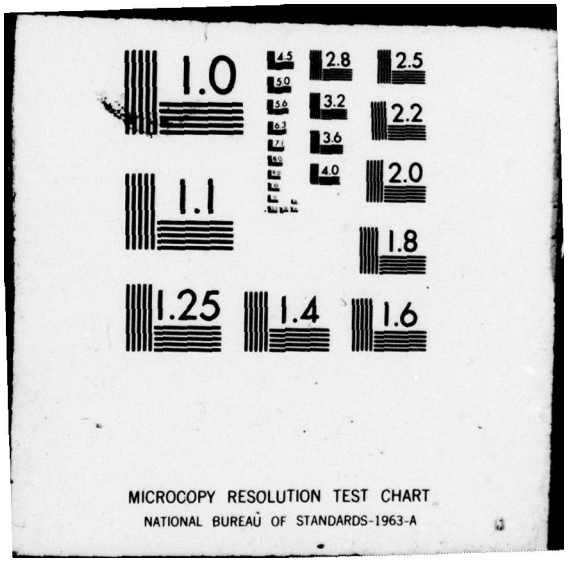
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

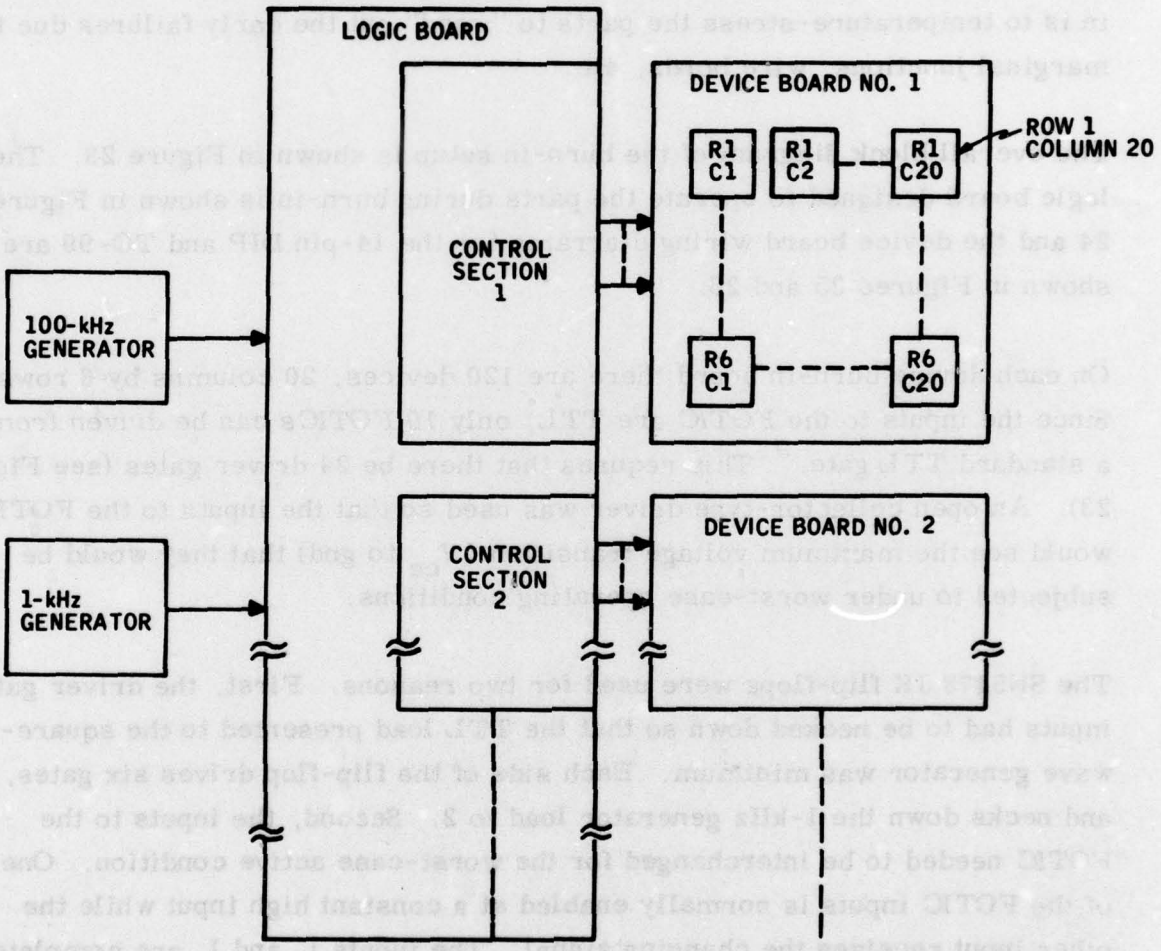


Figure 23. Burn-In Setup Block Diagram

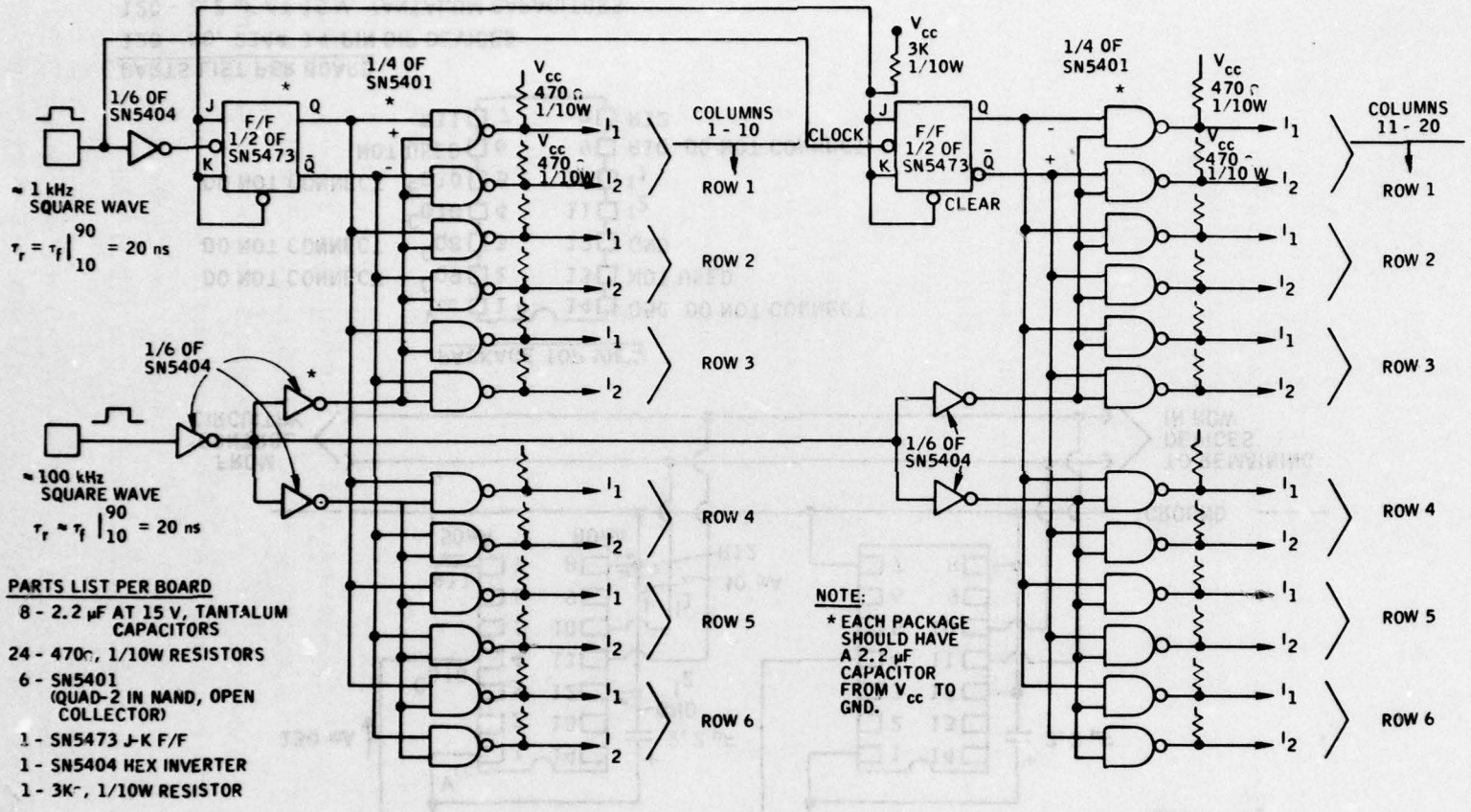
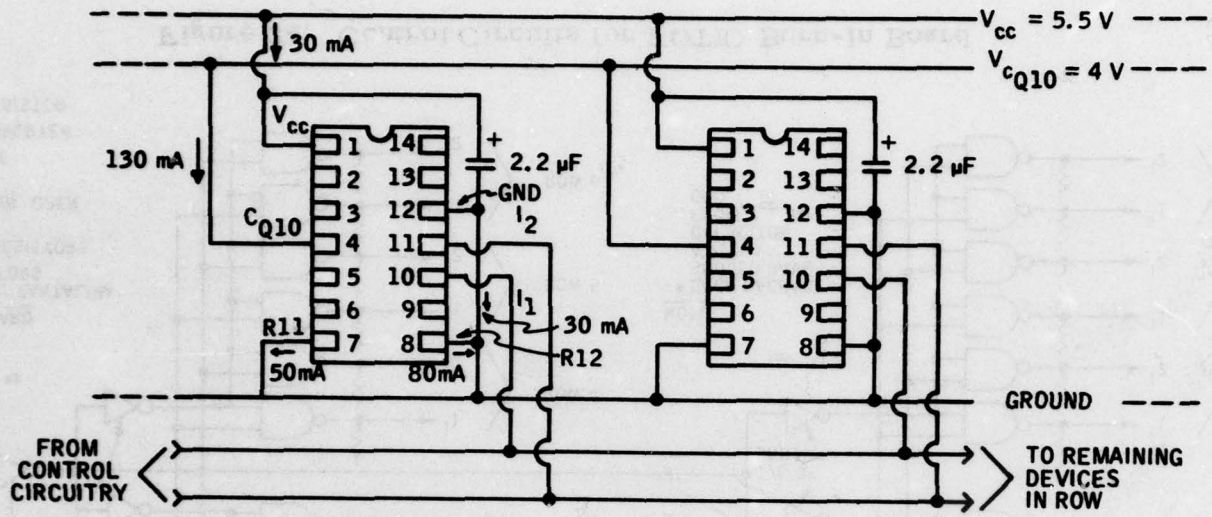


Figure 24. Control Circuits for FOTIC Burn-In Board



PACKAGE TOP VIEW

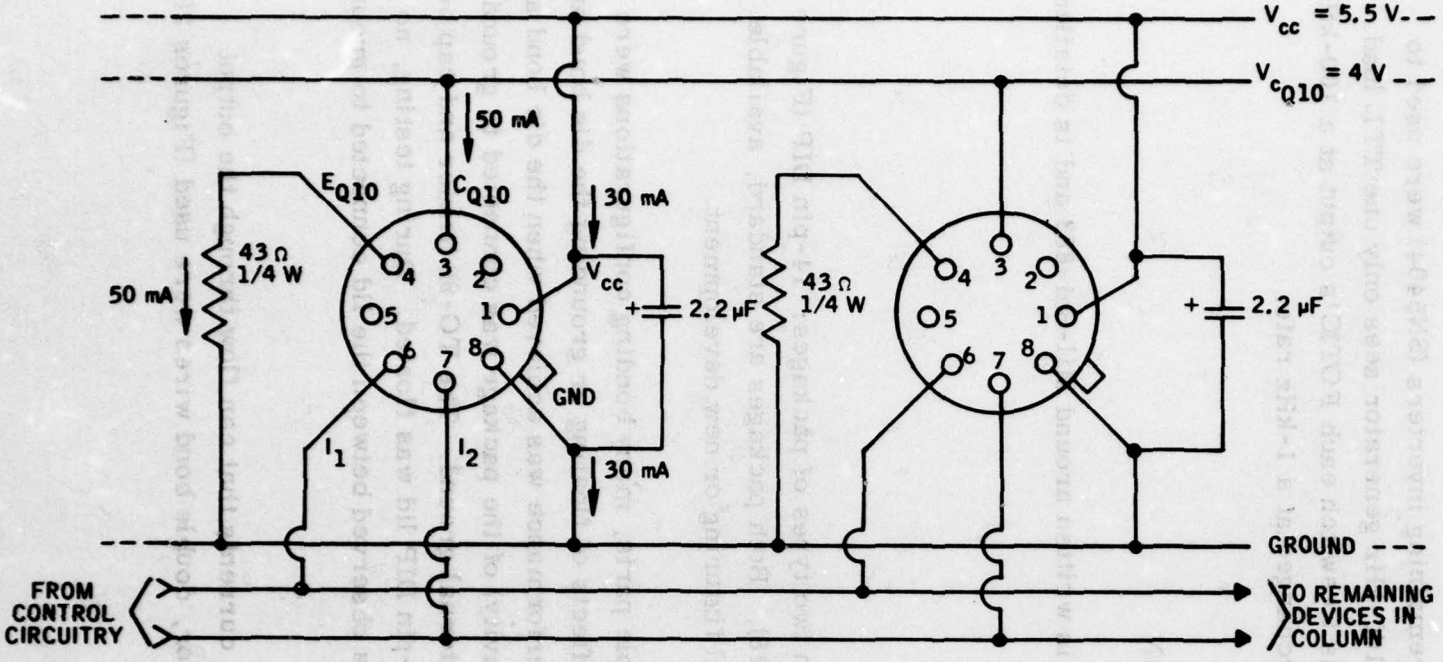
	V_{cc} 1	14	Q5E	DO NOT CONNECT
DO NOT CONNECT	C_{Q9} 2	13	NOT USED	
DO NOT CONNECT	C_{Q8} 3	12	GND	
	C_{Q10} 4	11	I_2	
DO NOT CONNECT	E_{Q10} 5	10	I_1	
NOT USED	6	9	R10	DO NOT CONNECT
	R11 7	8	R12	

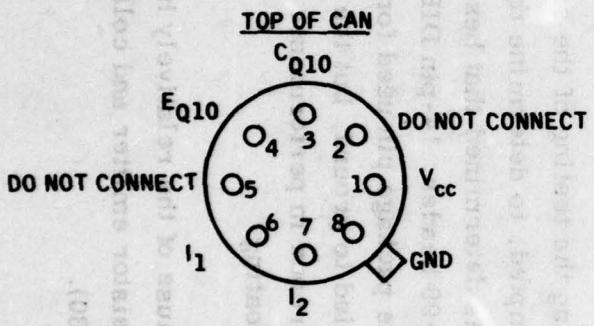
PARTS LIST PER BOARD

120 - NO. 2144 14-PIN DIP DEVICES

120 - 2.2 µF AT 15 V, TANTALUM CAPACITORS

Figure 25. 14-Pin DIP Device No. 2144 Burn-In Circuit





PARTS LIST PER BOARD

120 - NO. 2144 TO-99 DEVICES
120 - HEAT SINKS
120 - 43 Ω, 1/4W RESISTORS
120 - 2.2 μF AT 15 V, TANTALUM CAPACITORS

Figure 26. 8-Pin TO-99 Device No. 2144 Burn-In Circuit

uses I_2 as the enable). The remaining inverters (SN5404) were used to neck down the loading so the 100-kHz generator sees only one TTL load. The idea of the control logic is to switch each FOTIC's output at a 100-kHz rate while its inputs are interchanged at a 1-kHz rate.

FOTIC QUALIFICATION PLAN

The FOTIC qualification plan is written around Mil-Std-883 and is detailed in Table 37.

PACKAGING

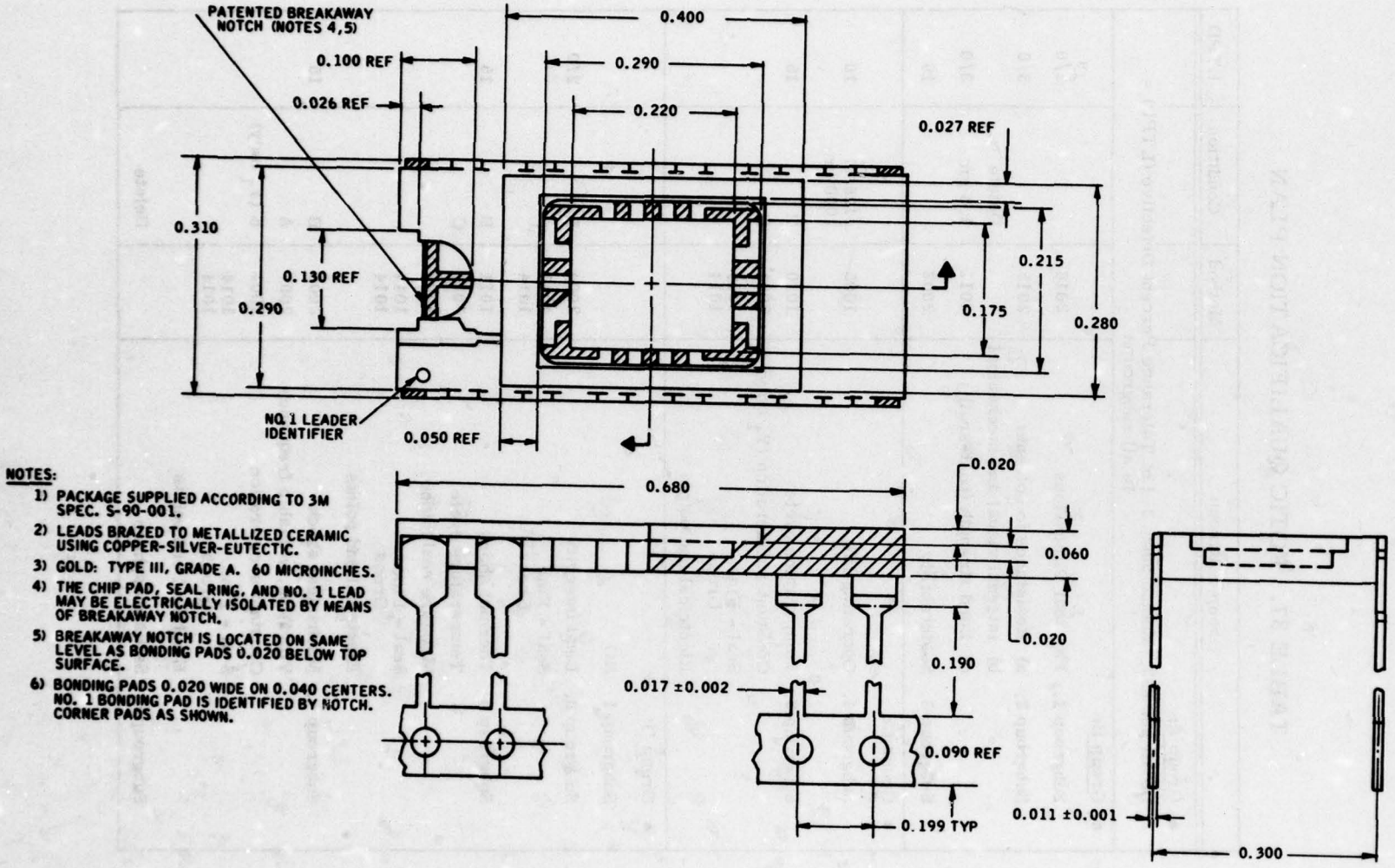
The FOTICs were packaged in two types of packages: 14-pin DIP (Figure 27) and 8-pin TO-99 (Figure 28). Both packages are standard, available types, and required no special fixturing or new development.

During the testing of the sample parts, many bonding configurations were attempted, to determine the effects of floating or grounding the die bond area. It was determined that best performance was achieved when the die bond area (TO-99 header, 14-pin DIP cavity) of the package was connected to ground at the package pin used for external ground. The TO-99 header and cap both get tied to ground, but the 14-pin DIP lid was floated. During testing, no difference in performance was observed between the lid connected to ground or floating.

Because of the relatively high currents that can flow through the output transistor emitter and collector, double bond wires were used (Figures 29 and 30).

TABLE 37. FOTIC QUALIFICATION PLAN

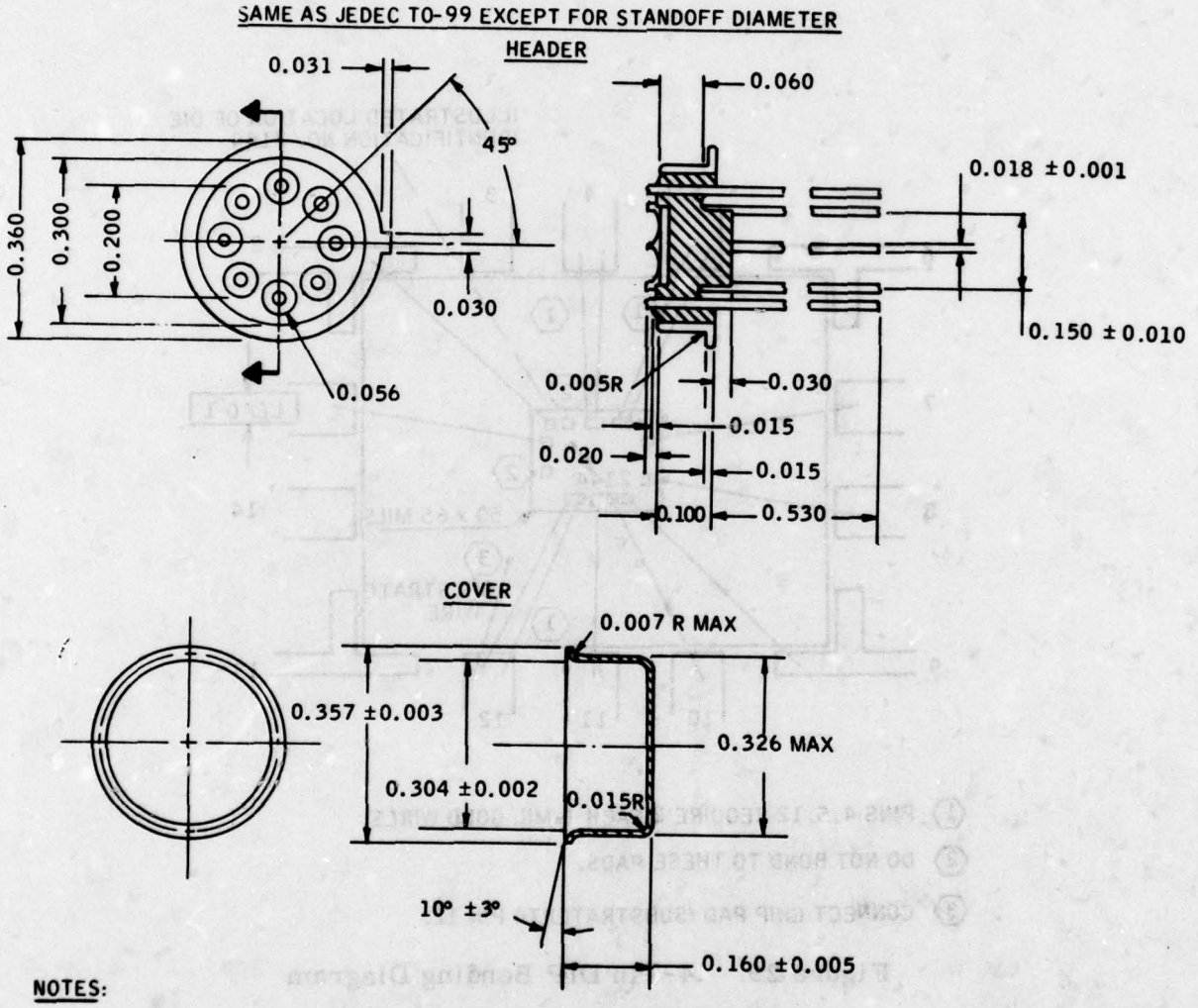
Group/Subgroup		Method	Condition	LTPD
• Group A:				
Do all per 883, Method 5005.3 Lot Tolerance Percent Defective (LTPD) = 10 all subgroups				
• Group B:				
Subgroup 1.	Physical Dimensions	2016		2/0
Subgroup 2.	a) Resistance to solvents	2015		3/0
	b) Internal visual and mechanical		Delete	
	c) Bond strength (post-seal)	2011	1.5 gm	3/0
Subgroup 3.	Solderability	2003		15
• Group C:				
Subgroup 1.	Operating life	1005	+125°C 1000 hr	10
Subgroup 2.	Temperature cycle	1010	C	15
	Constant acceleration (Y_1 only)	2001	D	
	Seal - Fine	1014		
	Gross	1014		
	Electrical end points			
• Group D:				
Subgroup 1.	NO			
Subgroup 2.	Lead integrity	2004	B_2	2/0
	Seal - Fine	1014		
	Gross	1014		
Subgroup 3.	Thermal shock	1011	B	15
	Temperature cycle	1010	C	
	Moisture resistance	1004		
	Seal - Fine	1014		
	Gross	1014		
	Electrical end points			
Subgroup 4.	Mechanical shock	2002	B	15
	Vibration, variable frequency	2007	A	
	Constant acceleration	2001	E (Y_1 only)	
	Seal - Fine	1014		
	Gross	1014		
	Electrical end points			
Subgroup 5.	Salt atmosphere		Delete	



NOTES:

1) PACKAGE SUPPLIED ACCORDING TO 3M SPEC. S-90-001.
2) LEADS BRAZED TO METALLIZED CERAMIC USING COPPER-SILVER-EUTECTIC.
3) GOLD: TYPE III, GRADE A. 60 MICROINCHES.
4) THE CHIP PAD, SEAL RING, AND NO. 1 LEAD MAY BE ELECTRICALLY ISOLATED BY MEANS OF BREAKAWAY NOTCH.
5) BREAKAWAY NOTCH IS LOCATED ON SAME LEVEL AS BONDING PADS 0.020 BELOW TOP SURFACE.
6) BONDING PADS 0.020 WIDE ON 0.040 CENTERS. NO. 1 BONDING PAD IS IDENTIFIED BY NOTCH. CORNER PADS AS SHOWN.

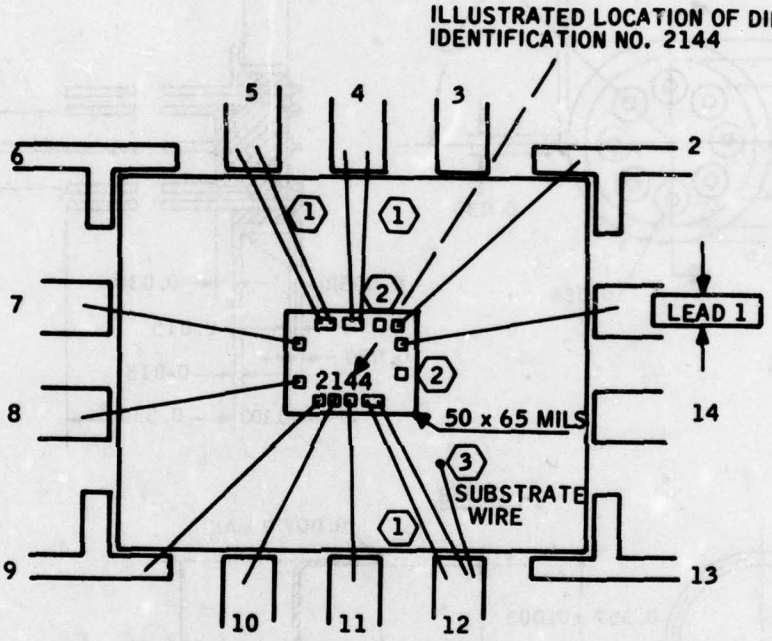
Figure 27. 14-Pin Ceramic Dual-In-Line Package



NOTES:

1) FINISH: GOLD PLATE, 80 MICROINCHES (MINIMUM) OVER ALL HEADER SURFACES BY BETA METHOD.
2) COVER MATERIAL: 0.012 GRADE A NICKEL, TYPE 200.
3) MATERIAL: BASE AND PINS - KOVAR.
4) GLASS FEED-THROUGHS TO BE OPAQUE.
5) WIRE BOND SURFACE FLAT WITHIN 0.001 FOR 0.012 DIA. MIN.

Figure 28. 8-Pin TO-99 Can



(1) PINS 4,5,12 REQUIRE 2 EACH 1-MIL GOLD WIRES.

(2) DO NOT BOND TO THESE PADS.

(3) CONNECT CHIP PAD (SUBSTRATE) TO PIN 12.

Figure 29. 14-Pin DIP Bonding Diagram

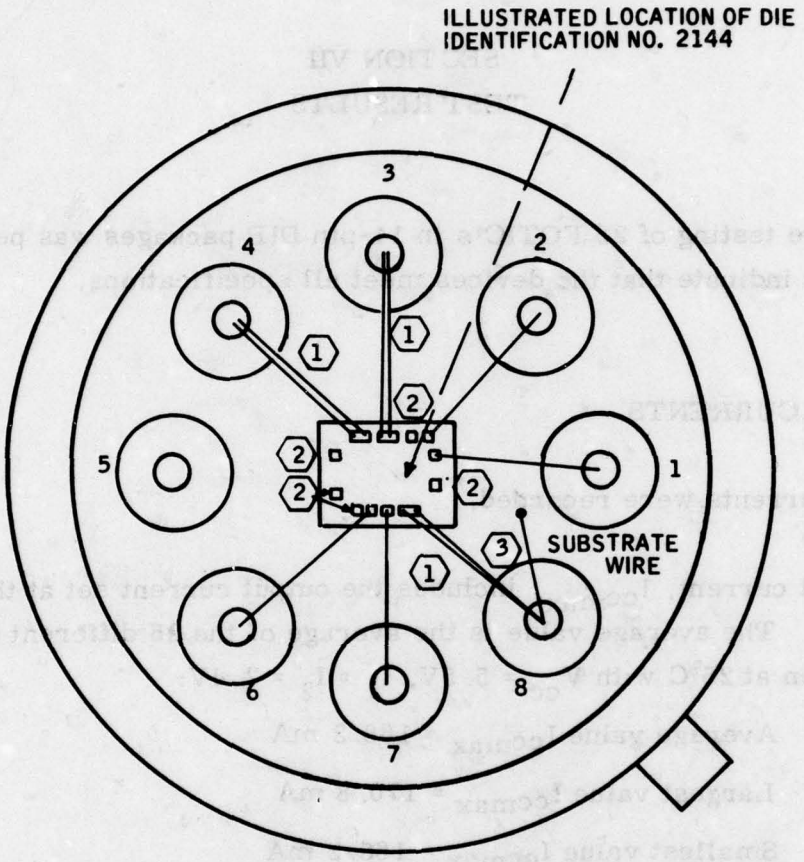


Figure 30. 8-Pin TO-99 Bonding Program

Although the ground lead wire bond only carries the relatively small chip current and not the LED current, double-wire bonds were used to reduce the inductance because the switching rate is quite fast in the TTL gate portion of the FOTIC.

SECTION VII
TEST RESULTS

Extensive testing of 26 FOTIC's in 14-pin DIP packages was performed. The data indicate that the devices meet all specifications.

DEVICE CURRENTS

Three currents were recorded.

The total current, I_{ccmax}, includes the output current set at the 150-mA position. The average value is the average of the 26 different device readings taken at 25°C with V_{cc} = 5.5V, $I_1 = I_2$ = 2.4V:

- Average value I_{ccmax} = 168.2 mA
- Largest value I_{ccmax} = 170.8 mA
- Smallest value I_{ccmax} = 166.2 mA

The ON current, I_{ON}, excludes I_{LED}. Data were taken at three temperatures with V_{cc} = 5.5V, $I_1 = I_2$ = 2.4V. Results are presented in Table 38.

TABLE 38. "ON" CURRENT TEST RESULTS

Parameter	-55°C	+25°C	+125°C	Units
Average value, I_{ON}	17.32	18.34	20.7	mA
Largest value, I_{ON}	18.08	18.89	21.5	mA
Smallest value, I_{ON}	16.60	17.88	20.0	mA

The OFF current, I_{OFF}, includes I_{LED}. Data were taken under the same conditions as for I_{ON}. Results are presented in Table 39.

TABLE 39. "OFF" CURRENT TEST RESULTS

Parameter	-55°C	+25°C	+125°C	Units
Average value, I_{OFF}	29.2	31.74	32.2	mA
Largest value, I_{OFF}	30.0	32.56	32.9	mA
Smallest value, I_{OFF}	28.4	31.43	31.4	mA

INPUT CURRENTS

Two input currents were measured for each input at two temperatures.

For the input low "0" state current measurement, V_{cc} = 5.5V, and the measured input was held at 0.4V with the other input at 2.4V. The two inputs were then reversed and the measurement repeated. Results are presented in Table 40.

TABLE 40. INPUT CURRENT TEST RESULTS

Parameter		-55°C	+125°C	Units
Average value	I_1 = 0.4V, I_2 = 2.4V	1.106	0.893	mA
	I_1 = 2.4V, I_2 = 0.4V	1.103	0.889	mA
Largest value	I_1 = 0.4V, I_2 = 2.4V	1.186	0.923	mA
	I_1 = 2.4V, I_2 = 0.4V	1.182	0.920	mA
Smallest value	I_1 = 0.4V, I_2 = 2.4V	1.081	0.875	mA
	I_1 = 2.4V, I_2 = 0.4V	1.079	0.873	mA

For the input high state current measurement, V_{cc} = 5.5V, and the measured input was held at 5.5V with the other input at GND. The two inputs were reversed and the measurement repeated. Some devices were damaged because proper filtering of the 5.5V input supply was not used and the input spiked up to 8V. Results are presented in Table 41.

TABLE 41. INPUT HIGH STATE CURRENT TEST RESULTS

Parameter		-55°C	+125°C	Units
Average value	---	0.17	17.58	μA
	---	0.24	18.67	μA
Largest value	---	0.39	39.9	μA
	---	0.76	41.7	μA
Smallest value	---	0.02	8.13	μA
	---	0.04	7.92	μA

INPUT THRESHOLD

The input threshold was defined as the voltage on the input that caused 1 mA to flow in the output with V_{cc} = 5.5V. The input not being measured was held at 2.4V. Because the data were taken at descrete points (0.7V, 0.8V, 0.9V) on the input, the actual voltage at threshold for -55°C and +125°C was not recorded. However, all devices had a threshold greater than 0.9V at -55°C and greater than 0.8V at +125°C. The values listed below are for +25°C.

- Average value, V_{TH} = 1.159V
- Largest value, V_{TH} = 1.180V
- Smallest value, V_{TH} = 1.147V

OUTPUT CURRENTS

Figure 31 shows the results of the data taken on the output current at three temperatures and two supply values for three current settings (50 mA, 100 mA, 150 mA). The ideal current is indicated for each of the three curves, as well as the average value at two supply voltages. The largest and smallest currents are also shown. Note that all the data points fall within ±5 percent of the ideal current.

SWITCHING CHARACTERISTICS

Measurements were taken on the switching characteristics at V_{cc} = 5V for three temperatures and three output current settings (50 mA, 100 mA, 150 mA). Input, I_1 was held at 2.4V and the input signal applied to I_2. The input signal had a 4-ns rise and fall and a 2.4V amplitude. Table 42 gives data for four typical devices at three temperatures and three output current settings. Results were as follows:

- Slowest rise time was 4.6 ns at +125°C, 150 mA.
- Fastest rise time was 3.1 ns at -55°C, 50 mA.
- Slowest fall time was 3.2 ns at +125°C, 50 mA.
- Fastest fall time was 1.9 ns at -55°C, 100 mA.
- Longest delay time was 8.1 ns at +125°C, 150 mA.
- Shortest delay time was 4.4 ns at -55°C, 50 mA.
- Largest distortion was 1.1 ns at 25°C, 50 mA.

Figures 32, 33, and 34 are oscilloscope pictures showing actual waveforms of input and output for device No. 10 at three temperatures and three output current settings. The output waveform is the voltage waveform of the output transistor emitter.

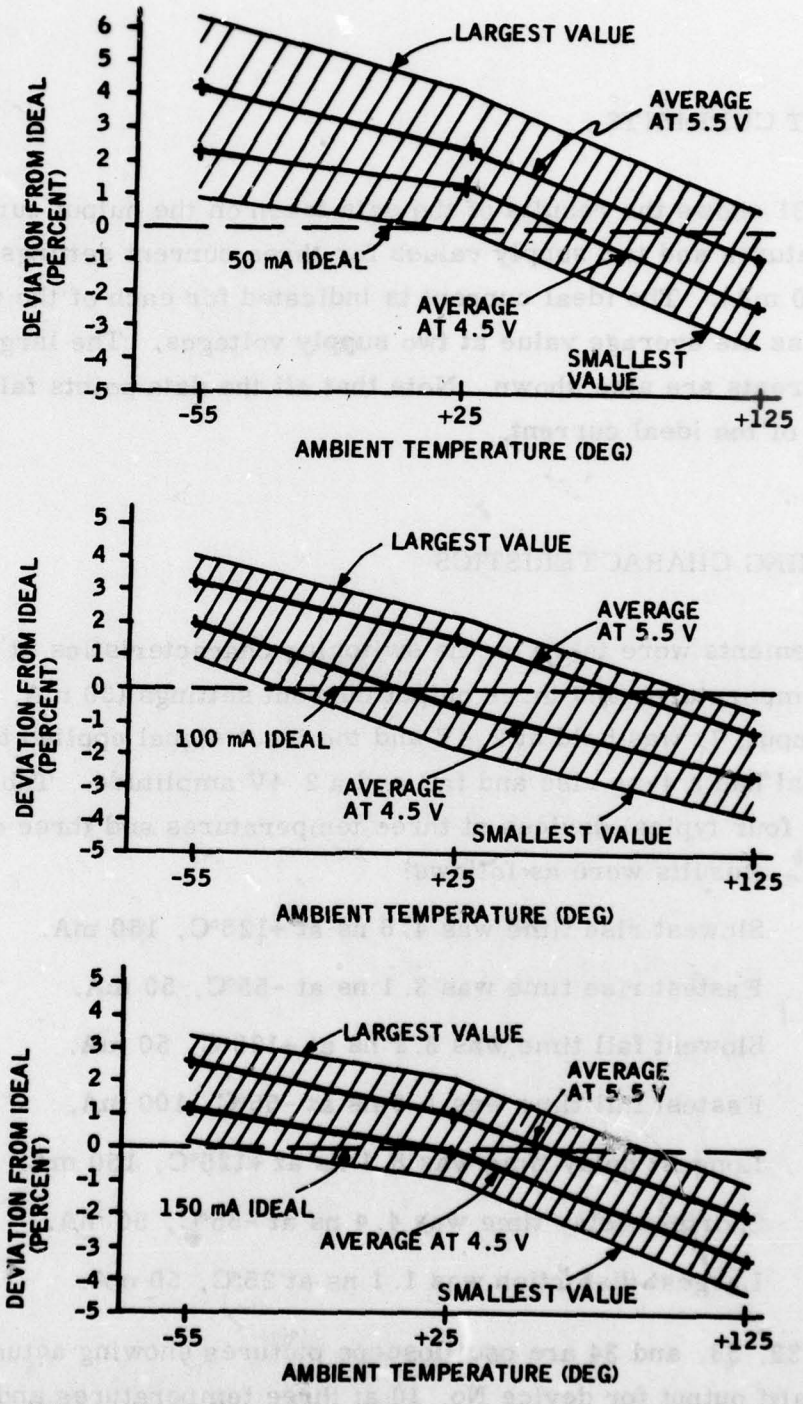


Figure 31. Deviation From Ideal LED Current

TABLE 42. SWITCHING TIMES

Parameter Name	Symbol[a]	I_{LED} at -55°C			I_{LED} at +25°C			I_{LED} at +125°C			Units
		50	100	150	50	100	150	50	100	150	mA
Device No. 8											
Rise time	$T_{O_{LH}}$	3.1	3.2	3.5	3.1	3.3	3.7	3.4	3.3	4.2	ns
Fall time	$T_{O_{HL}}$	2.4	1.9	2.0	2.7	2.3	2.3	3.2	2.6	2.6	ns
Delay rise	$T_{D_{LH}}$	4.5	4.4	4.6	5.5	5.6	5.9	6.8	7.1	7.5	ns
Delay fall	$T_{D_{HL}}$	5.3	5.2	5.3	5.4	5.4	5.5	7.2	7.2	7.3	ns
Distortion	$\lvert T_2-T_1 \rvert$	0.8	0.4	0.7	0.1	0.2	0.4	0.4	0.1	0.2	ns
Device No. 9											
Rise time	$T_{O_{LH}}$	3.1	3.1	3.2	3.2	3.6	3.7	3.4	3.6	4.1	ns
Fall time	$T_{O_{HL}}$	2.5	1.9	2.0	2.8	2.6	2.3	3.2	2.6	2.7	ns
Delay rise	$T_{D_{LH}}$	4.4	4.4	4.6	5.1	5.2	5.5	7.4	7.7	8.1	ns
Delay fall	$T_{D_{HL}}$	5.1	5.1	5.2	5.8	5.8	5.9	7.2	7.2	7.4	ns
Distortion	$\lvert T_2-T_1 \rvert$	0.7	0.7	0.6	0.7	0.6	0.4	0.2	0.5	0.7	ns
Device No. 10											
Rise time	$T_{O_{LH}}$	3.1	3.2	3.5	3.2	3.6	3.7	3.4	3.7	4.3	ns
Fall time	$T_{O_{HL}}$	2.3	1.9	2.1	2.6	2.4	2.4	3.2	2.6	2.7	ns
Delay rise	$T_{D_{LH}}$	4.4	4.4	4.6	4.8	4.9	5.2	6.9	7.1	7.6	ns
Delay fall	$T_{D_{HL}}$	5.3	5.2	5.4	5.8	5.8	5.9	7.1	7.2	7.3	ns
Distortion	$\lvert T_2-T_1 \rvert$	0.9	0.8	0.8	1.0	0.9	0.7	0.2	0.1	0.3	ns
Device No. 11											
Rise time	$T_{O_{LH}}$	4.0	3.4	3.7	3.1	3.3	3.7	3.5	3.8	4.6	ns
Fall time	$T_{O_{HL}}$	3.0	2.2	2.1	2.6	2.2	2.2	2.7	2.7	2.9	ns
Delay rise	$T_{D_{LH}}$	4.8	4.4	4.6	4.7	4.9	5.2	6.7	7.0	7.4	ns
Delay fall	$T_{D_{HL}}$	5.8	5.2	5.3	5.8	5.8	5.9	7.0	7.1	7.2	ns
Distortion	$\lvert T_2-T_1 \rvert$	1.0	0.8	0.7	1.1	0.9	0.7	0.3	0.1	0.2	ns

[a]Refer to Section III, Figure 3 for definition of symbols.

Conditions:

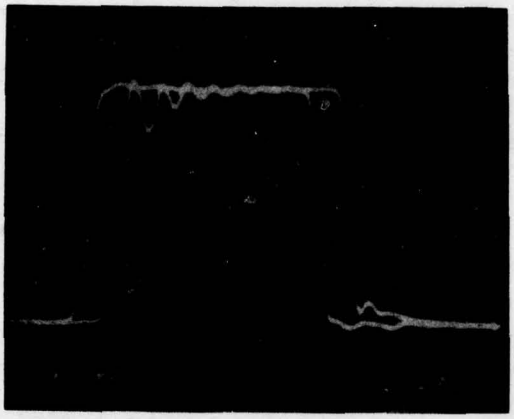
a) V_{cc} = 5.5V.

b) I_1 = 2.4V, I_i = signal.

c) Input signal defined by Figure 3 had 4-ns rise and fall.

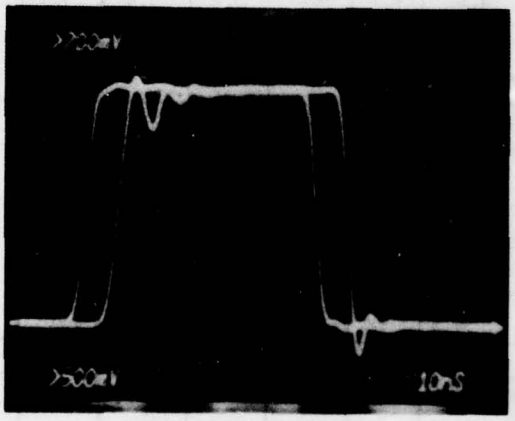
d) I_{LED} values are ideal, not actual.

CONDITIONS: V_{cc} = 5.5V, I_1 = 2.4V, I_2 = SIGNAL
TEMPERATURE = +25°C



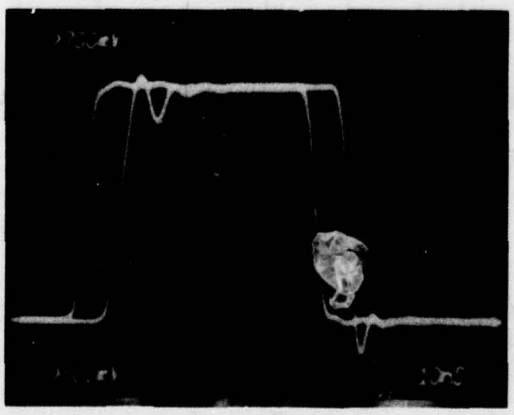
I_{LED} = 50 mA

$T_{O_{LH}}$ = 3.4 ns
$T_{O_{HL}}$ = 3.2 ns
$T_{D_{LH}}$ = 6.9 ns
$T_{D_{HL}}$ = 7.1 ns
$/T_2-T_1/$ = 0.2 ns



I_{LED} = 100 mA

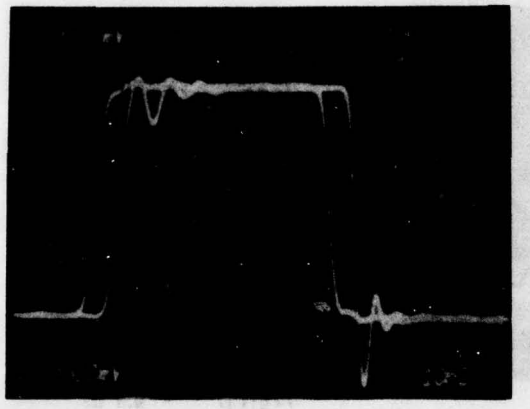
$T_{O_{LH}}$ = 3.7 ns
$T_{O_{HL}}$ = 2.6 ns
$T_{D_{LH}}$ = 7.1 ns
$T_{D_{HL}}$ = 7.2 ns
$/T_2-T_1/$ = 0.1 ns



I_{LED} = 150 mA
$T_{O_{LH}}$ = 4.3 ns
$T_{O_{HL}}$ = 2.7 ns
$T_{D_{LH}}$ = 7.6 ns
$T_{D_{HL}}$ = 7.3 ns
T_2-T_1 = 0.3 ns

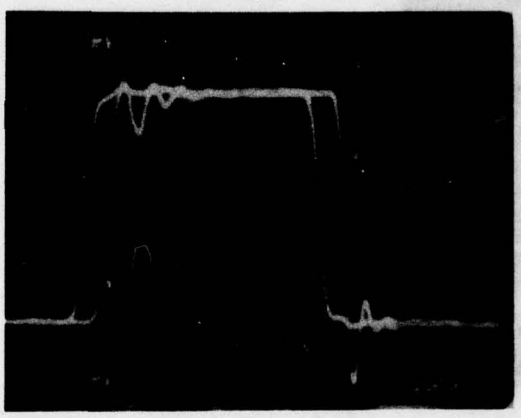
Figure 32. FOTIC Input/Output Waveforms

CONDITIONS: V_{cc} = 5.5V, I, = 2.4V, I_2 = SIGNAL
TEMPERATURE = +125°C



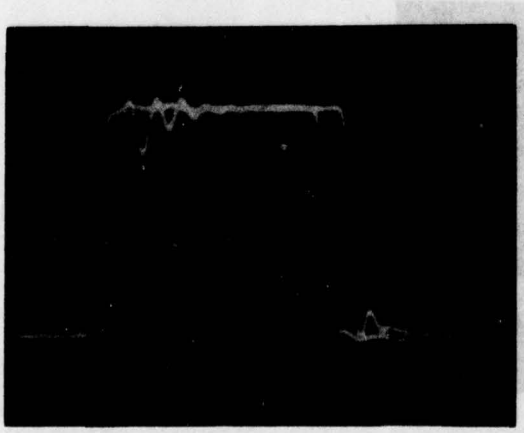
I_{LED} = 50 mA

$T_{O_{LH}}$ = 3.2 ns
$T_{O_{HL}}$ = 2.6 ns
$T_{D_{LH}}$ = 4.8 ns
$T_{D_{HL}}$ = 5.8 ns
$/T_2 - T_1/$ = 1.0 ns



I_{LED} = 100 mA

$T_{O_{LH}}$ = 3.6 ns
$T_{O_{HL}}$ = 2.4 ns
$T_{D_{LH}}$ = 4.9 ns
$T_{D_{HL}}$ = 5.8 ns
$/T_2 - T_1/$ = 0.9 ns

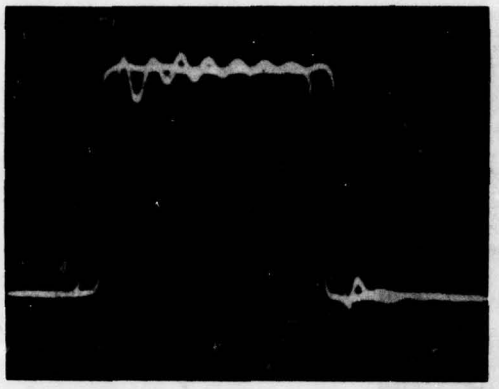


I_{LED} = 150 mA

$T_{O_{LH}}$ = 3.7 ns
$T_{O_{HL}}$ = 2.4 ns
$T_{D_{LH}}$ = 5.2 ns
$T_{D_{HL}}$ = 5.9 ns
$T_2 - T_1$ = 0.7 ns

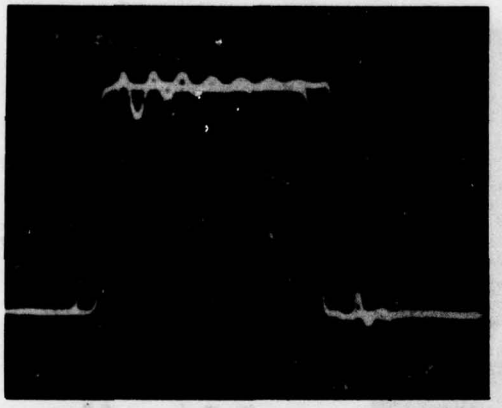
Figure 33. FOTIC Input/Output Waveforms

CONDITIONS: V_{cc} = 5.5V, I, = 2.4V, I_2 = SIGNAL
TEMPERATURE = -55°C



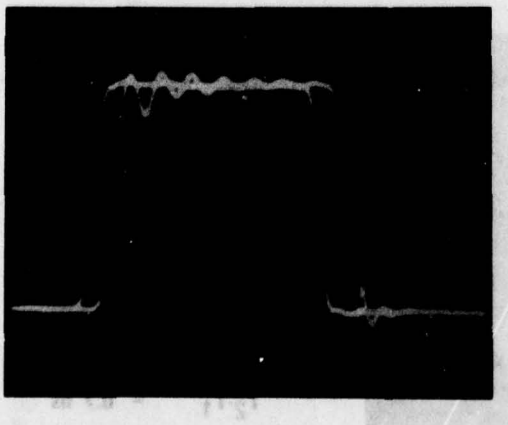
I_{LED} = 50 mA

$T_{O_{LH}}$ = 3.1 ns
$T_{O_{HL}}$ = 2.3 ns
$T_{D_{LH}}$ = 4.4 ns
$T_{D_{HL}}$ = 5.3 ns
$/T_2-T_1/$ = 0.9 ns



I_{LED} = 100 mA

$T_{O_{LH}}$ = 3.2 ns
$T_{O_{HL}}$ = 1.9 ns
$T_{D_{LH}}$ = 4.4 ns
$T_{D_{HL}}$ = 5.2 ns
$/T_2-T_1/$ = 0.8 ns



I_{LED} = 150 mA

$T_{O_{LH}}$ = 3.5 ns
$T_{O_{HL}}$ = 2.1 ns
$T_{D_{LH}}$ = 4.6 ns
$T_{D_{HL}}$ = 5.4 ns
T_2-T_1 = 0.8 ns

Figure 34. FOTIC Input/Output Waveforms

APPENDIX

ADVANCED BIPOLAR PROCESS DESCRIPTION

The Honeywell Advanced Bipolar Process I (ABP-I) is the current standard bipolar process used for all internal Honeywell needs. Devices built using this process are used in Honeywell's large and small computers, and in various commercial and industrial sensor and control electronics, as well as classified military applications.

A brief description of the processing sequence follows. The cross-sectional views of Figure A-1 show the various diffused and implanted regions and the oxide layers used to control the etching and junction formations. The top views of Figure A-2 show the actual masks used to obtain the profiles shown in Figure A-1. Although the processing steps allow for other components (resistors, diodes, etc.) to be formed at the same time in the surface of the same wafer, both figures show only a single transistor for clarity.

The processing begins by oxidizing the surface of a polished P-type wafer to form a masking oxide layer. The first mask (buried layer, Figure A-2.1) is used to define the pattern in the oxide layer. Then the N^+ dopant is diffused into the wafer to form the buried layer (Figure A-1.1). A lightly doped N epitaxial layer (epi) is then grown and a thin layer of silicon dioxide (SiO_2) grows on top of it while the N^+ Buried Layer diffuses up into it (Figure A-1.2). The silicon nitride (Si_3N_4) is then grown on top of the SiO_2, and the second mask is used to etch the patterns that will become the self-aligned isolation, sinker, and base regions (Figures A-1.3, A-2.2). In older processes, these three regions were defined with separate patterns. Since all three regions are defined by the same pattern, higher-performance (less capacitance) and higher-density transistors result.

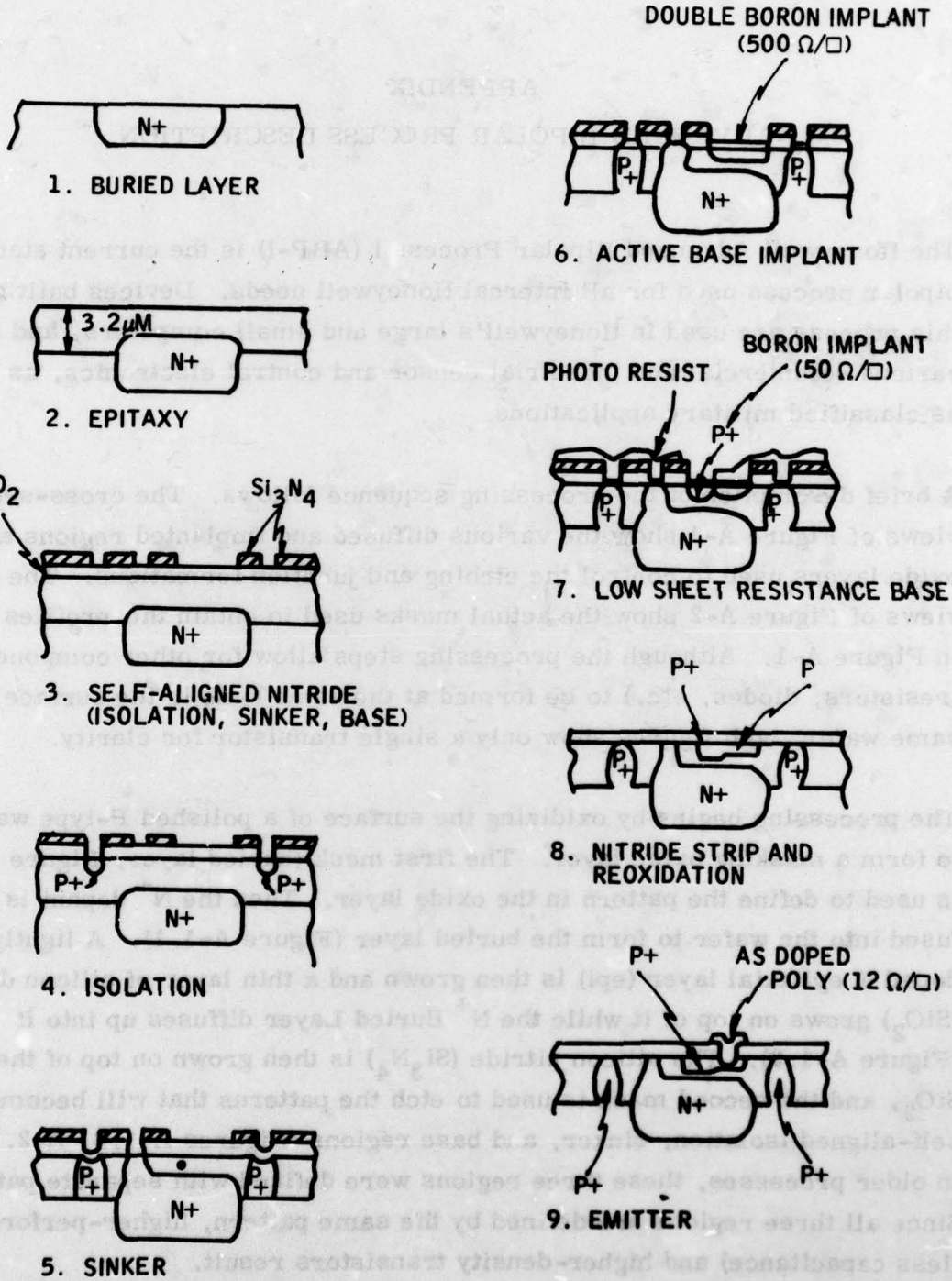


Figure A-1. Basic ABP I Processing Sequence

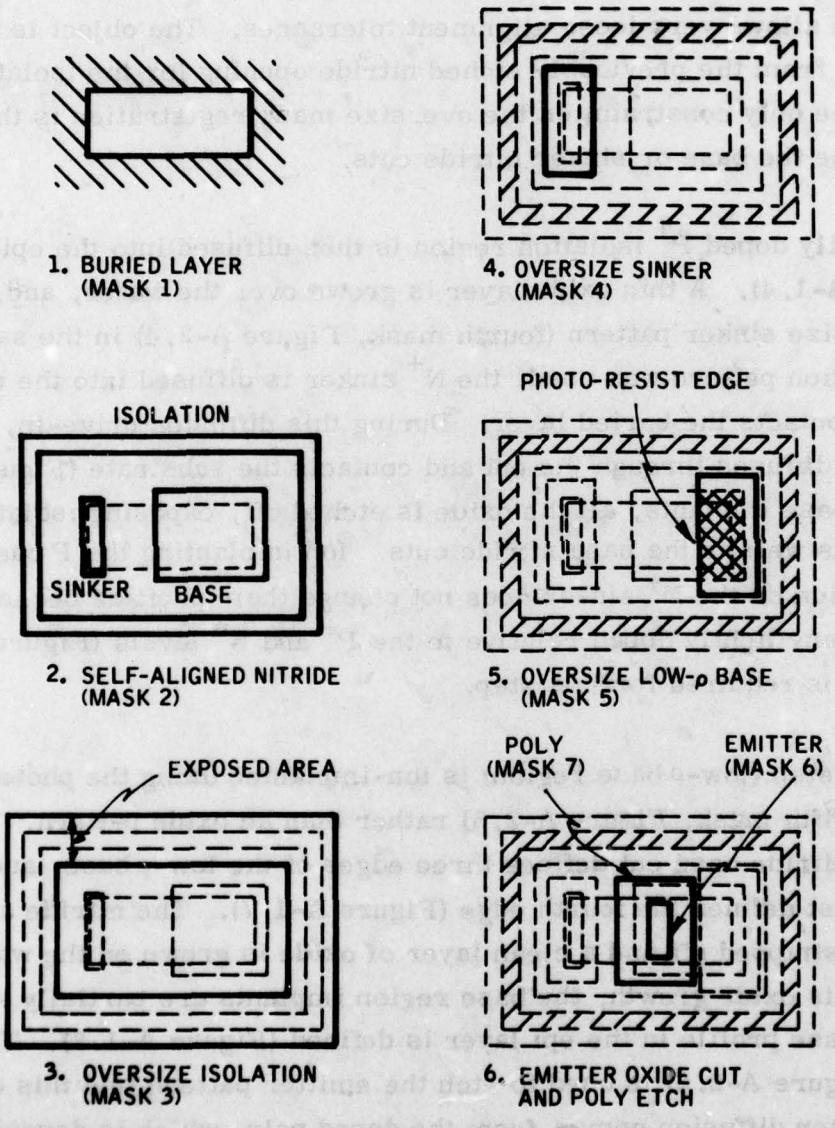


Figure A-2. Basic ABP I Masking Sequence

A thick SiO_2 layer is then grown over the nitride and the oversize isolation pattern (third mask, Figure A-2.3) is etched into it. This oversize mask technique allows very loose alignment tolerances. The object is to remove the oxide from the previously etched nitride opening for the isolation region only. The only constraint on the oversize mask registration is that it does not expose the base or sinker nitride cuts.

The heavily doped P^+ isolation region is then diffused into the epi layer (Figure A-1.4). A thin oxide layer is grown over the wafer, and, using the oversize sinker pattern (fourth mask, Figure A-2.4) in the same way the isolation pattern was used, the N^+ sinker is diffused into the epi layer until it contacts the buried layer. During this diffusion drive-in, the P^+ isolation diffuses through the epi and contacts the substrate (Figure A-1.5). For the base implants, all the oxide is etched off, exposing isolation and sinker, as well as the base nitride cuts. Ion implanting the P base into the P^+ isolation or the N^+ sinker does not change their profiles because the P base is very lightly doped relative to the P^+ and N^+ levels (Figure A-1.6). No mask is required for this step.

The next step (low-ρ base region) is ion-implanted using the photoresist pattern (fifth mask, Figure A-2.5) rather than an oxide pattern. Notice that the nitride base cut defines three edges of the low-ρ base, and the photoresist defines the fourth edge (Figure A-1.7). The nitride and oxide are then stripped off and a clean layer of oxide is grown on the wafer. During this oxide growth, the base region implants are partially annealed and the base profile in the epi layer is defined (Figure A-1.8). The emitter mask (Figure A-2.6) is used to etch the emitter pattern into this oxide. The emitter diffusion comes from the doped poly, which is deposited and then etched using the seventh mask (Figures A-1.9 and A-2.6). The remaining steps (contacts and metal) are not shown because they are standard processing steps well known to all semiconductor processing. Either single-metal or double-metal systems are available to be used to interconnect the various components diffused into the epi.

Some of the features that result from this processing sequence are:

- There is self-alignment through use of a silicon nitride cut that defines the field region. This feature allows for considerable simplification of the processing sequence, ultimately making the processing largely insensitive to photomask defects, etching errors, oxidation aberrations, etc. One further advantage of this technique is the ability of the nitride to ensure proper shielding of the field regions from the base implants.

- The base region is composed of a three-part boron implantation. This allows for the possibility of producing two independently adjustable base resistors. The key feature here is the use of a double-boron implant for the active transistor region (a deep implant for active characteristics, and a shallow one for sheet resistance purposes), and a heavier implant for a low-resistance inactive base (used to reduce r_b'). This arrangement allows the inactive base sheet resistance to be varied from 35 to 130 $\Omega/\square$, and the active base resistance to be varied from 350 to 1000 $\Omega/\square$.

- Photoresist shielding is used during the inactive base implant and greatly simplifies the processing by allowing for the use of only one implant oxidation.

- A polysilicon, arsenic-doped emitter allows for the elimination of the aluminum spiking problem inherent in shallow emitter structures. Also, by maintaining the emitter concentration at a high level ($10^{20}/cm^3$), advantage is taken of the concentration-enhanced diffusivity of arsenic to produce a narrow base region with a steep emitter-base profile. This

allows for better emitter efficiency, while maintaining the base push effect of phosphorous.

Figure A-3 gives the emitter-base-collector diffusion profile produced by this process. Notice the steep emitter doping gradient (for efficient injection), the relatively narrow base (for high-frequency response), and the

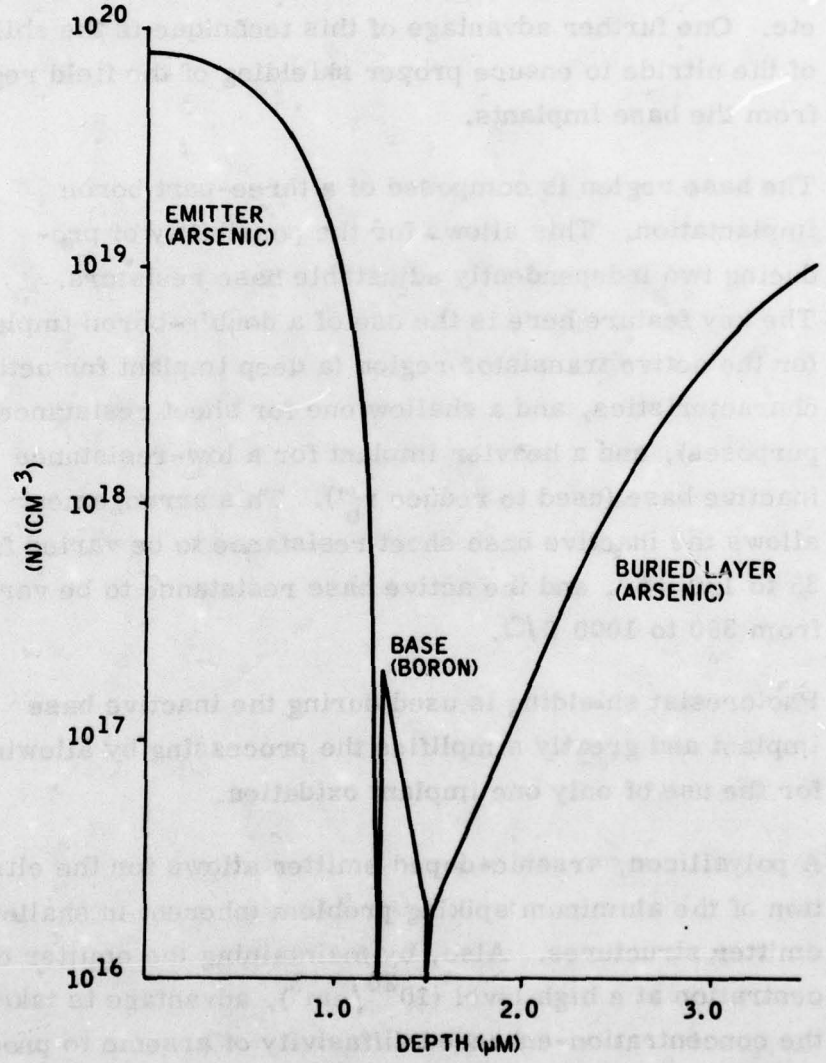


Figure A-3. The Emitter-Base Buried-Layer Doping Profile as Found From Spreading Resistance Measurements

proximity of the buried layer (for low saturation resistance). The intrinsic transit time of the base region is about 300 ps, as shown by the plot of $1/I_E$ versus $1/f_T$ (Figure A-4).

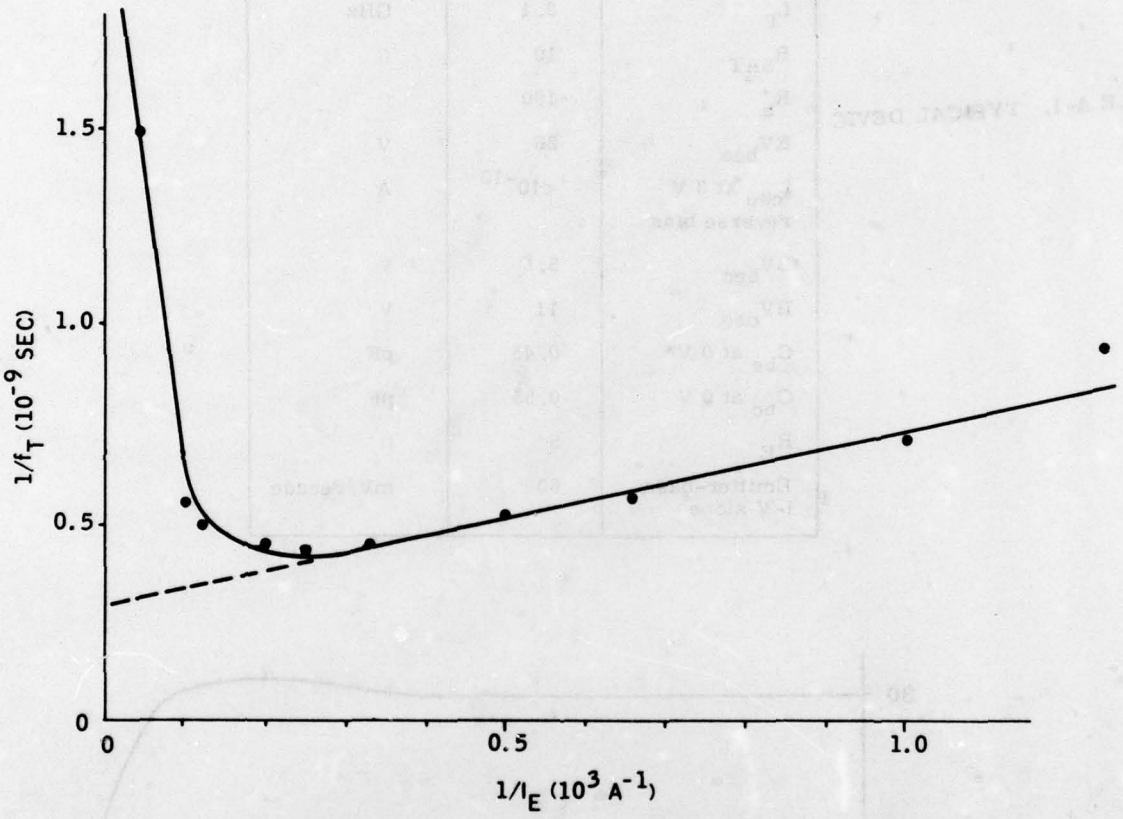


Figure A-4. $1/f_T$ versus $1/I_E$

The basic transistor produced by this process is approximately 60 percent smaller than the older non-self-aligned processes, while the devices are intrinsically faster. Typical device parameters are listed in Table A-1. One of the most striking features of this process is the production of a flat β versus I_E curve over several decades (Figure A-5). This feature is due to a general predominance of the diffusion current over the recombination current at all current levels greater than 10^{-10} A.

TABLE A-1. TYPICAL DEVICE PARAMETERS

Parameter	Value	Units
H_{fe}	80	
f_T	2.1	GHz
R_{SAT}	10	Ω
R_b'	190	Ω
BV_{bco}	25	V
I_{cbo} at 3 V reverse bias	$<10^{-10}$	A
BV_{beo}	5.6	V
BV_{ceo}	11	V
C_{be} at 0 V	0.45	pF
C_{bc} at 0 V	0.55	pF
R_E	5	Ω
Emitter-base I-V slope	60	mV/decade

TABLE A-1. TYPICAL DEVIC

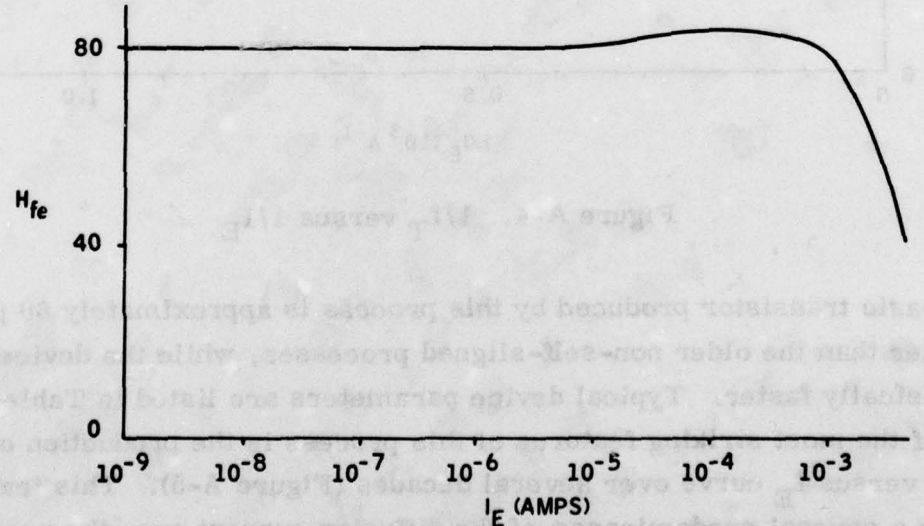


Figure A-5. H_{fe} versus I_E

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